Discussion Section 8

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Dynamic CMOS Power

- Switching CMOS devices takes power
  - Need current to charge/discharge gate capacitances
- Power vs. performance tradeoff
  - More capacitance = more power
  - Faster speed = more power
  - Higher voltage = more power

Dynamic CMOS Power

$$P_{sw} = \frac{1}{2}\alpha C V_{DD}^2 F$$

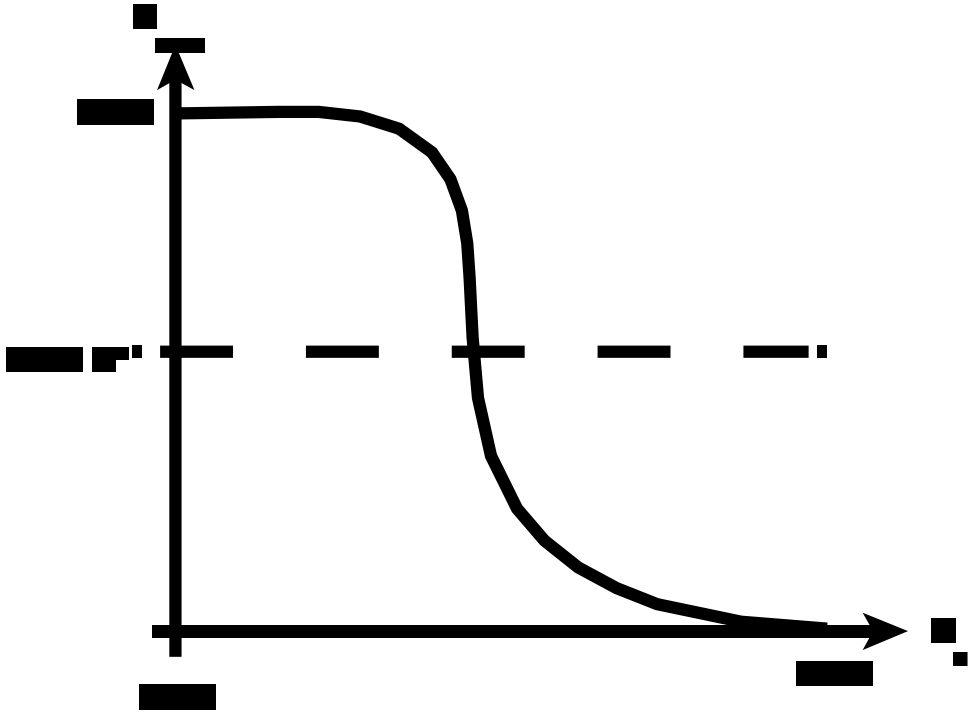
- Switching power depends on device characteristics and operating voltage/frequency
  - Device characteristics determined by foundry and technology node
  - Voltage and Frequency most easily variable for designers
  - Capacitance can be optimized with layout and routing/simplification
- Can design around α
  - Design logic paths so they do not switch as often -> less power
  - Some paths must have α=1 (e.g clock)

Dynamic Power Example

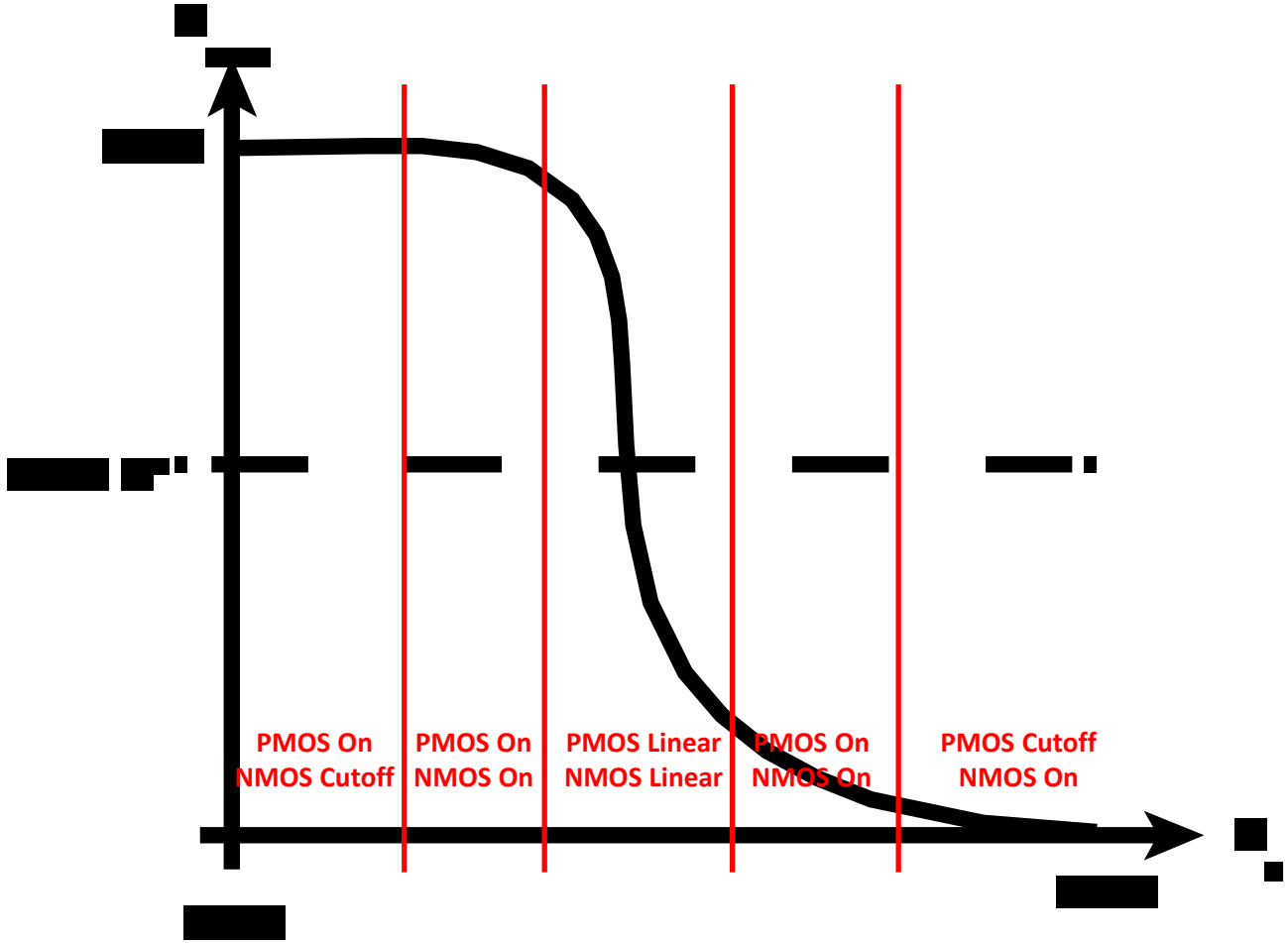
- VDD = 1V, f = 3.8GHz
- C_{in} = 30fF (x2 to take wires into account)

Short-Circuit CMOS Power

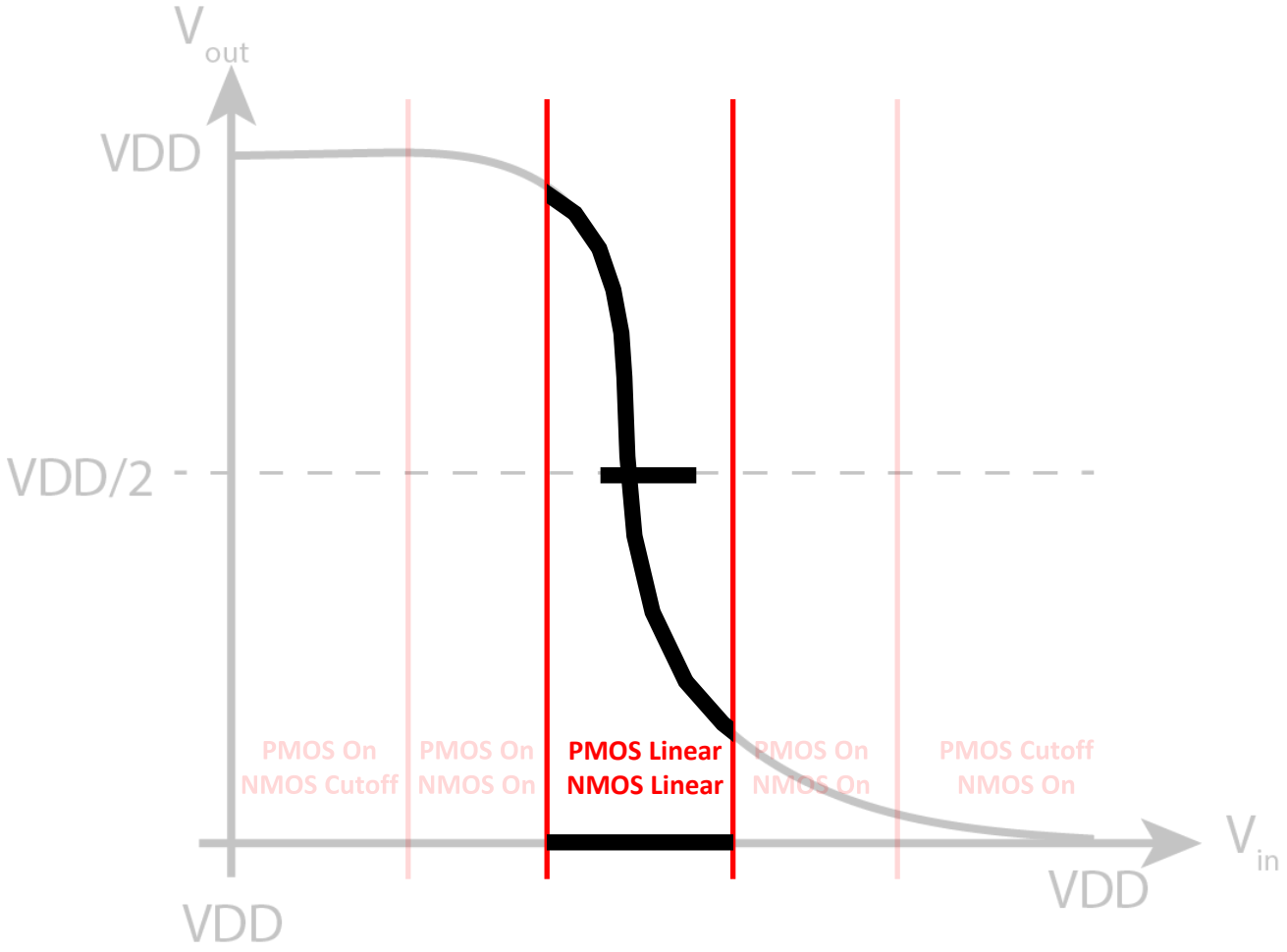
- Transient power from switching
- Faster transitions mean less SC power (less time for current)



Short-Circuit CMOS Power



Short-Circuit CMOS Power

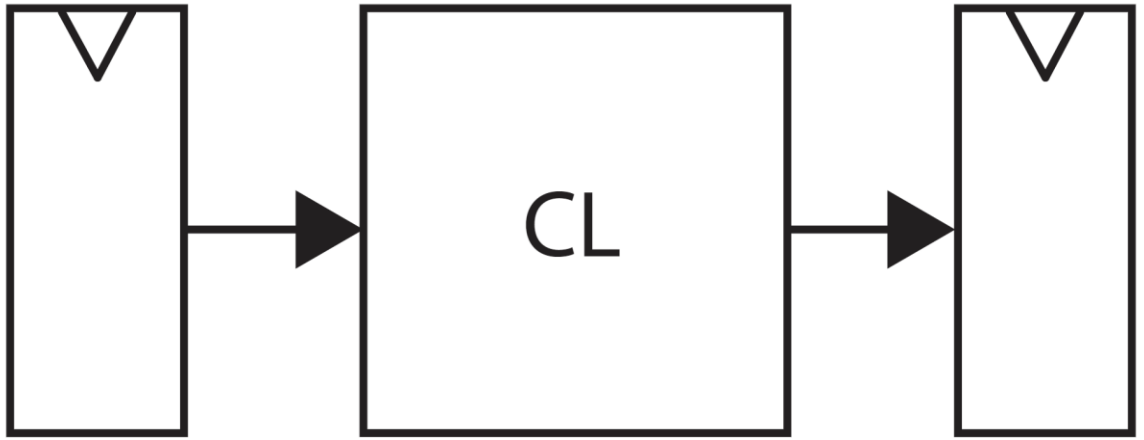


Leakage CMOS Power

- Transistor in cutoff mode not really off!
  - Transistors are solid-state devices
  - Cutoff transistors only present extremely high (but not infinite) resistance
  - Basically “always-on” short circuit power!
- Modern planar devices hard to truly turn off
  - Short channel effects and reduced gate control over channel
  - New techniques to try to mitigate this (FinFET, SOI, GAA)
- Gate leakage
  - Modern planar device oxide thickness very thin

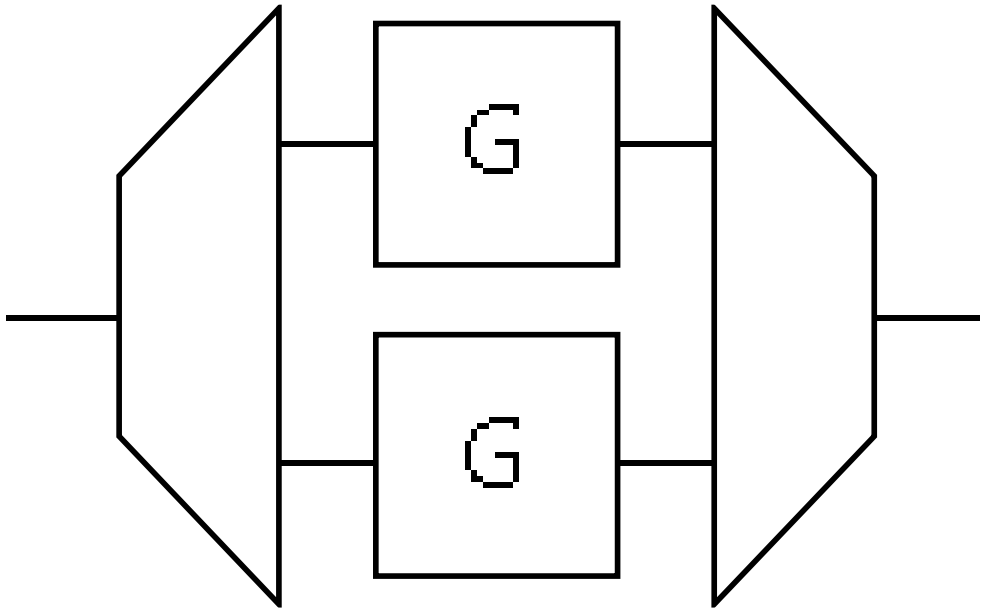
Pipelining

- Can divide datapath into sequential “checkpoints”
  - Divides critical path into shorter paths
  - Can run at same frequency but lower supply voltage

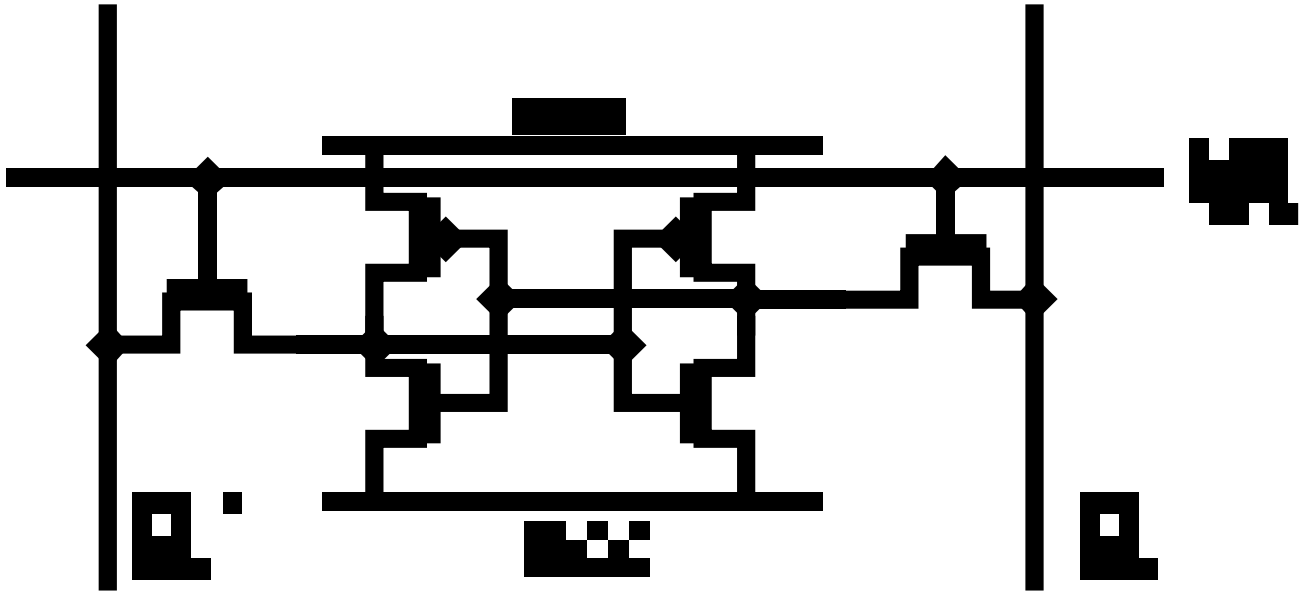


Parallelization

- Copy logic and run two together
- Can run at lower clock frequency and have same throughput from hardware replication

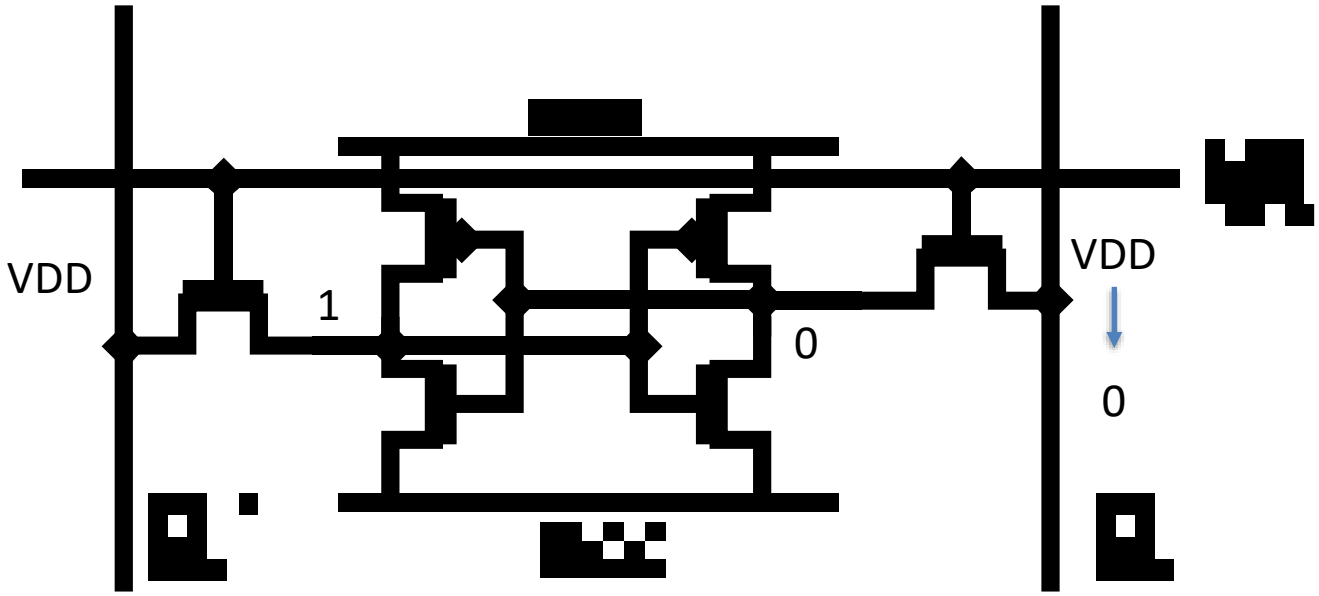


SRAM Cells



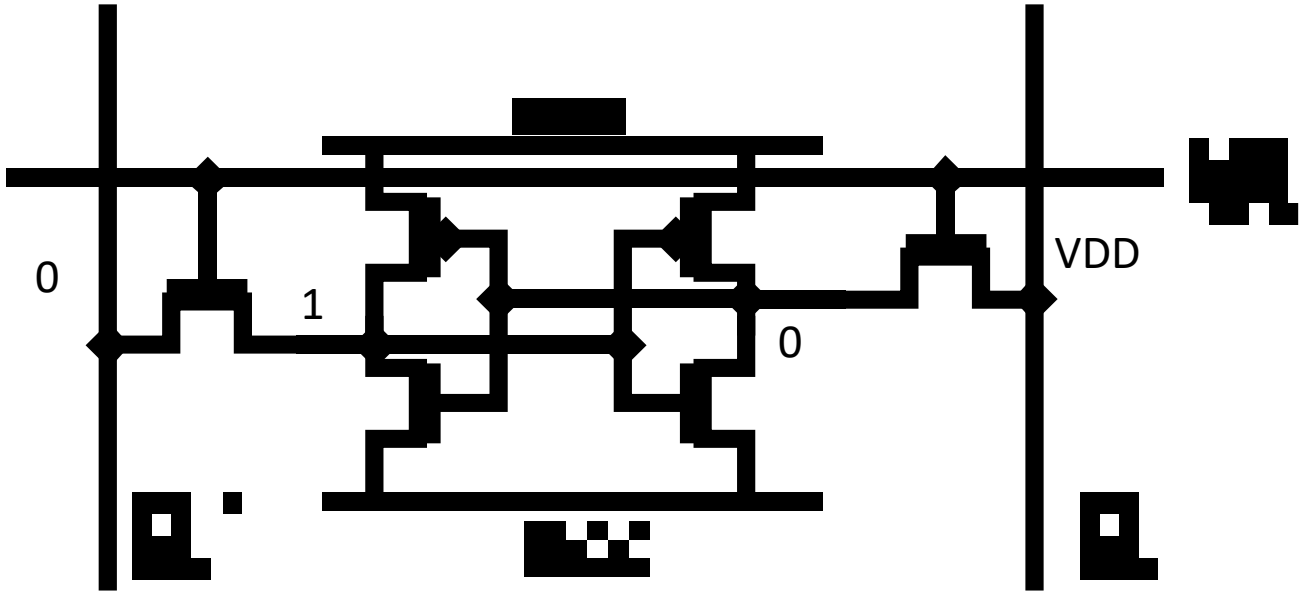
- 6T SRAM
  - Back-to-back inverters hold value (latch)
  - Access transistors to read/write from SRAM

SRAM Read



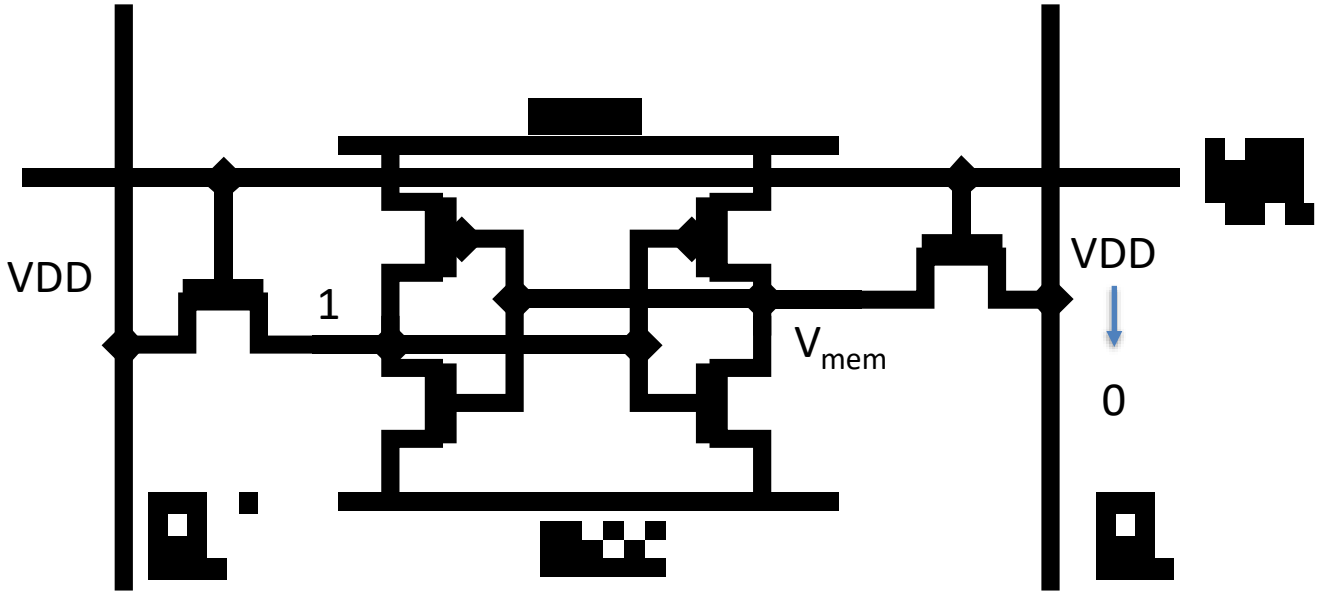
1. Bit lines both pre-charged to VDD
2. Word line pulled high to open access transistors
3. Side holding 0 will pull the bit line down and this change in voltage is measured
   - Side not holding 0 is unchanged

SRAM Write



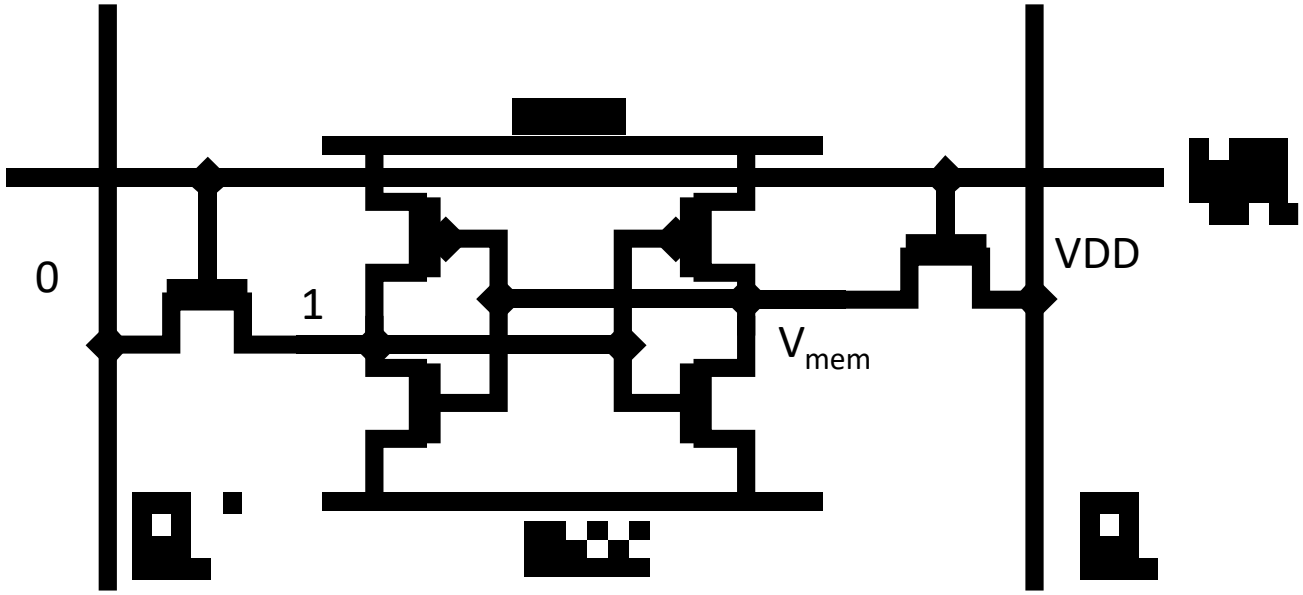
1. Bit lines both pre-charged to value to be written
2. Word line pulled high to open access transistors
3. Bit line must overpower value held by latch to write new value

SRAM Sizing for Read



- V_{mem} should not cross switching voltage (e.g. VDD/2) to avoid corrupting memory
- Access transistor should be smaller than memory cell transistors

SRAM Sizing for Write



- V_{mem} must be driven beyond switching voltage
  - Below VDD/2 for writing 0, above VDD/2 for writing 1
- Access transistor must be larger than memory cell transistors