EECS 151/251A Exam 1 Information

Exam Date: Mar 11, 2021

The exam will be a "take home exam" and take place Thursday March 11, 6–9PM. The exam comprises a set of questions with 1 point per expected minute of completion with a total of approximately 120 points. 251A students will be asked to complete extra questions. All students are allowed to refer to your notes, the class lecture notes, and any other reference materials that you have available. However, the problems are challenging and if you are not suitable familar with the course topics, you may not have much time to look at notes. Except for course staff, you are not allowed to speak or communicate with anyone on any topic related to the course during the exam period. After completing the exam, you will be asked to sign a statement attesting that you did not discuss or otherwise communicate with anyone regarding the exam. You will turn in your answers with Gradescope as you do your homework.

We will be using zoom to proctor and answer questions you might have. Details of setting us zoom will be provided in a seperate document.

Topics:

1. Moore's Law Definition and Consequences
2. Dennard Scaling and Consequences
3. Cost/Performance/Power Design Tradeoffs and Pareto Optimality
4. NRE and Recurring costs for ICs
5. Definitions and representations of combinational logic
6. Principle of restoration
7. Basic principle behind edge-triggered clocking and RTL design methodology
8. Digital system implementation technology alternatives and relative strengths and weaknesses
9. FPGA versus ASIC cost analysis

10. Principle behind structural versus behavioral hardware description
11. Basic Verilog descriptions for combinational logic
12. Verilog generators blocks
13. Verilog instantiation of state elements
14. Simple sequential circuits using registers (counters for instance)
15. FPGA reconfigurable fabric architecture
16. Details of FPGA fabric interconnect switches
17. Details of FPGA logic blocks with LUT
18. Logic circuit partitioning for and mapping to FPGA fabric
19. Ripple Adder Circuits
20. Laws of Boolean algebra
21. Boolean algebra representation of logic circuit and manipulation
22. Canonical forms
23. K-map method for 2-level logic simplification
24. Multi-level logic circuits
25. Bubble-pushing method for converting from AND/OR to NAND/NOR
26. FSM state transition diagram (STD) representation
27. FSM implementation in circuit based on STD
28. FSMs description in Verilog
29. FSM Moore versus Mealy styles
30. FSM one-hot encoding design method
31. Basics of planar CMOS IC processing
32. Basics of transistor and wire layout
33. IC manufacturing trends and scaling

34. Static switch-level complementary CMOS logic gates
35. Transmission-gate logic circuits
36. Tri-state buffers
37. Edge-triggered Flip-flop implementation and operation
38. Maximum clock frequency calculation from circuit parameters
39. Origin of gate-delay and calculation
40. Delay property of wires and rebuffering
41. Circuit register rebalancing
42. Logic delay combined with wires
43. Driving large capacitive loads
44. Delay calculations for simple logic gates