EECS 151/251A Final Exam Information

Exam Date: May 14th, 2021

The exam will be a "take home exam" and take place Friday May 14, 7–10PM. The exam comprises a set of questions with 1 point per expected minute of completion with a total of approximately 120 points. 251A students will be asked to complete extra questions. All students are allowed to refer to your notes, the class lecture notes, and any other reference materials that you have available. However, the problems are challenging and if you are not suitable familar with the course topics, you may not have much time to look at notes. Except for course staff, you are not allowed to speak or communicate with anyone on any topic related to the course during the exam period. After completing the exam, you will be asked to sign a statement attesting that you did not discuss or otherwise communicate with anyone regarding the exam. You will turn in your answers with Gradescope as you do your homework.

We will be using zoom to proctor and answer questions you might have. Details of setting us zoom will be provided in a seperate document.

Topics:

The final exam will be comprehensive and test all topics covered this semester. However, emphasis will be placed on topics covered after the midterm exam—those listed below.

1. How to Design a RISC-V Single-Cycle Processor from the ISA
2. Processor Pipelining Hazards and Mechanisms
3. Sources of Power and Energy consumption in Digital ICs
4. Principles Behind Six Low-power Design Techniques
5. How to Improve Energy Efficiency through Parallelism and Pipelining
6. Memory Block Internal Architecture
7. SRAM Cell and Read/Write Operation
8. Memory Block Periphery Circuits
9. Memory Decoder Design
10. DRAM Cell and Read/Write Operation
11. Dual-port Memory Architecture
12. Cascading Memory blocks for More Width, Depth, and Ports

13. FIFO Implementation
14. Serialization versus Parallelization in Iterative Computations
15. Principles of Pipelining and Restrictions of Loops
16. C-Slow Technique for Pipelining Loops
17. List Processor Design and Optimizations
18. Modulo Scheduling
19. Carry Select Adder Design
20. Carry Lookahead and Parallel Prefix Adders
21. Bit-Serial Addition
22. Array Multiplier Design
23. Carry Save Addition
24. Signed Multiplication
25. Bit-Serial Multiplication
26. CSD Multiplier Design
27. Booth Encoding
28. Log and Barrel Shifters Design and Analysis
29. Use of Counters in Controller Design
30. Effect of Clock Uncertainties on Maximum Clock Frequency and Race Margin
31. Source of Clock Uncertainties
32. Principle of Good Clock Distribution
33. IR and dI/dt effects in Power distribution
34. Types and Sources of Faults in ICs
35. Hamming Codes