EECS 151/251A Homework 1

Due Monday, Feb 1th, 2021

Problem 1: Pareto Optimal Frontier

John did a design space exploration for his design of a digital widget and came up with the following table of results for maximum frequency in GHz, energy efficiency in nanoJoules per operation, and cost as chip area in mm^2. List those rows that represent design points that lie on the Pareto optimal frontier.

f_{max}	Energy	Cost
2.0	20	2.0
1.5	10	1.5
1.5	17	1.5
1.5	20	1.0
1.0	10	1.5
1.0	20	1.0
1.0	10	1.5
0.2	5	1.0

Problem 2: Moore's Law Implications

Let's imagine an alternate history for a moment. Back in 1908, the Ford Motor Company introduced the Model T to the world as the first affordable automotive. This pioneering vehicle sported a 4-cylinder engine outputting 20 horsepower and came in any color you wanted as long as it was black! While working on developing the next generation of automobiles in 1910, one of the engineers at the company noticed that if they shrank the pistons in the engines of the cars, they could get the same performance out of the engine while using a leaner fuel-air mixture. This would mean each engine block could now fit even more pistons, and therefore output more power. Upon hearing of this, Henry Ford made the prediction that every 2 years the number of pistons in automobile engines would double, a notion that became known as "Ford's Law". Following this trend, how many pistons would today's gas-powered cars have if this were a real phenomenon in the automotive industry? Is this a realistic number of pistons to have in an engine? Barring the issues with sizing the piston (assume this world could make infinitesimally small pistons), what are some additional issues with having this many pistons in one engine?

Problem 3: Technology Survey

Take a look at your laptop/desktop computer. What processor is it using? Which technology node was it designed in (14 nm, 12 nm, 7 nm, etc.)? How many cores does it have? Does it have dedicated hardware accelerator blocks?

Problem 4: Die Cost

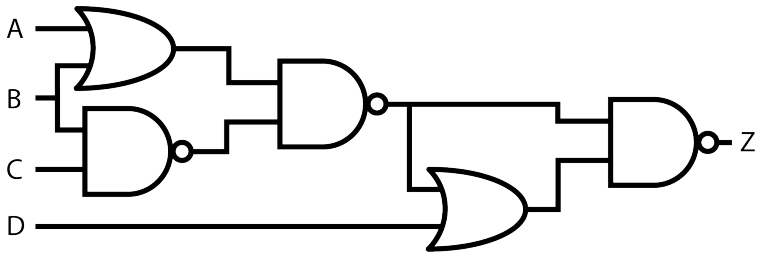
You want to fabricate 300 mm wafers with $\alpha = 3$ and a defect per unit area of 0.005 /mm^2.

(a) The die area is 25 mm^2 and the wafer cost is \$15k. What is your die yield and die cost?

(b) Your company is now pivoting to making FPGAs that are 500 mm^2 each, and the wafer costs have gone down so they are now \$8k each. What is your die yield and die cost?

Problem 5. Boolean Logic

For the digital logic circuit shown below, give the truth table.



Problem 6. Boolean Functions of 2 inputs

How many unique Boolean functions of 2 inputs exist? Give names for as many of them as you can, and write a Boolean expression for those you can't.

Problem 7: Rank order for NRE, Recurring Costs, Flexibilty, Performance

Rank order the following design alternatives by filling in the table with 1,2,3,4 representing the relative ranking (1 being the lowest and 4 being the highest). Rank based on the best-case design in each category. If there is a tie, use the lower number (e.g. if tied for 2 or 3, use 2)

	Full-Custom	Std Cell ASIC	Gate Array	FPGA
NRE Costs				
Max Performance				
Energy Efficiency				
Min Per Die Cost				
Flexibility				

Problem 8: FPGA vs. ASIC

You are the Chief Technical Officer of a new startup, the Citrus Scooter Company. As the chief design lead of your (admittedly small) team of engineers, it is up to you to choose whether to use

FPGAs or ASICs for your upcoming line of scooters. After getting quotes from several foundries and having a chat with the Head of HR about the estimated number of work hours needed for each choice, you arrive at the following conclusions for the NRE and per-die costs associated with each approach.

	NRE Cost	Per Die Cost
FPGA	\$25K	\$100
ASIC	\$14.75M	\$5

(a) As a small startup, you don't anticipate your first deployment to be too large, and the Head of Marketing (who also happens to be Head of HR) estimates that you will deploy about 3000 units in the first quarter. Which type of design would you choose? Why?

(b) After a successful launch, every city in the country is clamoring for the Citrus scooters! Soon your Head of Marketing comes into your office and excitedly tells you they promised to deploy 200,000 more units by next year. Would you want to switch strategies from your initial approach? If yes, what has now made the other approach so attractive?

(c) Upon doing some more analyses of the costs involved in switching from one to the other, you find that thankfully your staff have been very organized with their work and some parts can be converted over to the other type of design, which will incur the following NRE costs in converting the design (per-die costs remain the same).

	NRE Cost
FPGA to ASIC	\$12M
ASIC to FPGA	\$8K

How much would it cost to go from your original plan to the other? Is it worth it to switch now that the total cost will be cost of the first run + cost of converting? Is this better than having chosen the other option to begin with?

Problem 9: Voltage Transfer Curve (VTC) of Inverter in SPICE

Using SPICE DC Analysis, plot the VTC of an inverter using the 16nm process technology provided on `http://ptm.asu.edu/modelcard/LP/16nm_LP.pm`. The nominal supply voltage for this process is 0.9 V. Use a length of 16 nm for both devices and a width of 3 µm for PMOS and 1 µm for NMOS. Don't forget to connect the body of the devices to the correct voltages - NMOS body to GND and PMOS body to VDD!

Approximate the maximum voltage gain (slope of vout/vin). For help setting up the simulation, follow the LTspice tutorial on the class website. `https://inst.eecs.berkeley.edu/~eecs151/sp20/files/spice_tutorial.pdf`