

EECS 151/251A Homework 11

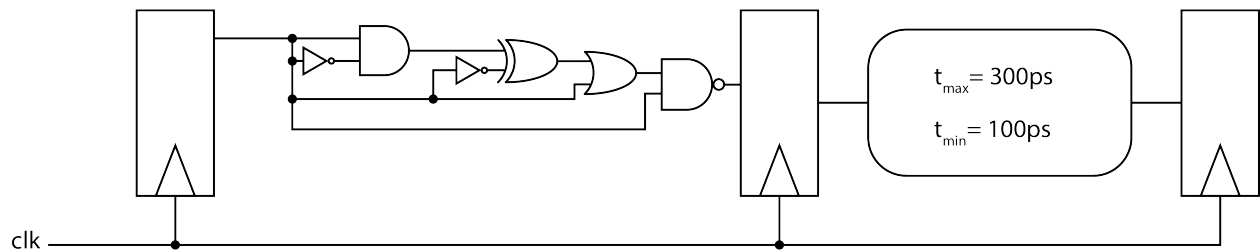
Due Monday, May 3th, 2021

For this Homework

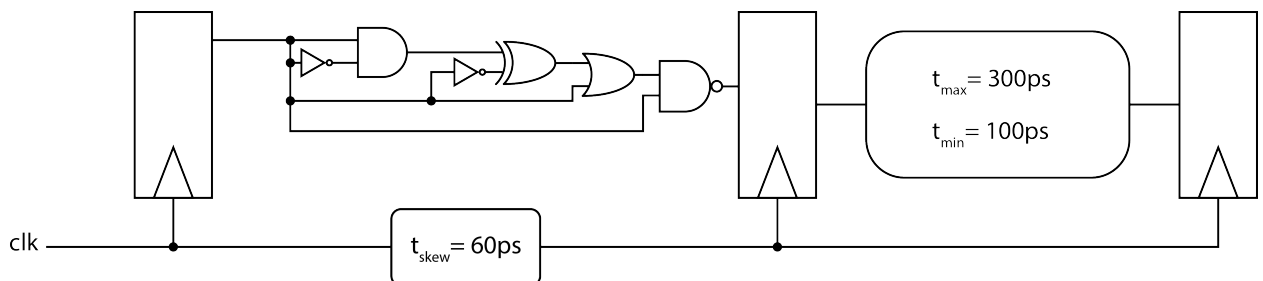
Please include a short (1-2 sentence) explanation with your answer, unless otherwise noted.

Problem 1: Timing

Consider the circuit below. All flip-flops have $t_{clk-q} = 40$ ps, $t_{setup} = 100$ ps. $t_{hold} = 80$ ps



- What is the maximum logic delay for the gate-level segment shown below if $t_{inv} = 30$ ps, $t_{AND} = 80$ ps, $t_{XOR} = 110$ ps, $t_{OR} = 100$ ps, $t_{NAND} = 50$ ps? What is the minimum logic delay?
- What is the maximum clock frequency of this circuit? Are there any potential hold time violations? If there are, draw a modified circuit fixing the hold time violation. You may add or subtract gates as long as the final result remains logically equivalent, but you may not modify the clock path or clock frequency.
- After performing the place and route, a clock skew has been added to the second register, as pictured below.



How does this affect your answers for part (a) and (b)? What is the new clock frequency? Has this now caused a hold time violation in another part of the circuit?

Problem 2: Error Correction Code

- (a) Encode the data bitstream 10011011 with Extended (SECDED) Hamming Code
- (b) The following bitstreams may contain some bit errors and are encoded with Extended (SECDED) Hamming Code. If there is a single error, identify the error bit and correct the bitstream. If there is a double error, identify that there is a double bit error. Otherwise, state that there is no error.
- 1001101010010
 - 0000101100101
 - 1110100101011

Problem 3: Faults

You are a circuit designer at PineApple, Inc., which makes consumer electronics. As part of the team designing the accelerometer chips present in every one of their myPhones, you are responsible for a rather large volume of chips all following your design. For each of the faults illustrated below, identify the type (design, manufacturing, runtime) and discuss their impact on costs for the company.

- (a) One day you get a call from the lead physical design engineer, who is responsible for assembling all the parts of the accelerometer before sending the final design to the fabrication facility. She notifies you that they managed to catch a bug in the Serial Peripheral Interface handler while they were performing final verification tests.
- (b) After the new myPhones have hit the market for a while, a sudden influx of customer service reports come in about the accelerometer. Curiously all of them seem to be phones that were sold within the last few months. After discussing the problem with the supply chain manager, you were able to trace all the problematic devices to a fabrication facility that recently had their photolithography machine sent in for maintenance due to some mask alignment issues.
- (c) You get a call from one of the retail stores where the workers there have encountered an error with the accelerometer that they can't explain. The customer came in complaining that their myPhone's accelerometer occasionally glitches, causing their phone to spontaneously change screen orientation. After asking for more details you discover that the customer in question had recently taken a round-trip trans-pacific flight to Japan.

Problem 4: Packaging

You have just finished finalizing the design for your newest processor. Your chip is designed to operate at 1.5 GHz, and in the worst case may experience current spikes of up to 15 A at 1 V for a period of 50 ps. After finishing your chip, you send the chip specifications to a packaging company, which gives you quotes on two methods of packaging.

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- (a) The bond wires on offer have a series inductance of 0.5 nH/mm , and each bond wire needs to be 5 mm long to reach the chip pads. How many bond wires would you need to keep the V_{DD} supply noise spike below 10% ?
- (b) The company also offers flip-chip solder ball attachment, which has a significantly reduced series inductance of 50 pH/mm , and are each about 1 mm long. How many solder balls would you need to achieve the same supply noise suppression as part (a)?