EECS 151/251A Homework 11

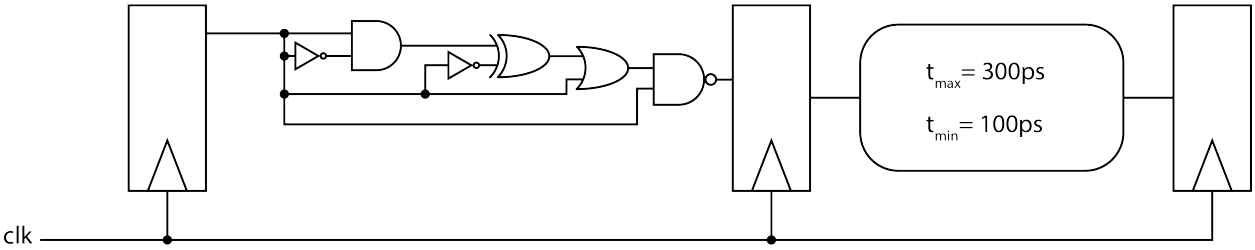
Due Monday, May 3th, 2021

For this Homework

Please include a short (1-2 sentence) explanation with your answer, unless otherwise noted.

Problem 1: Timing

Consider the circuit below. All flip-flops have $t_{clk-q} = 40\,\text{ps}$, $t_{setup} = 100\,\text{ps}$. $t_{hold} = 80\,\text{ps}$



(a) What is the maximum logic delay for the gate-level segment shown below if $t_{inv} = 30\,\text{ps}$, $t_{AND} = 80\,\text{ps}$, $t_{XOR} = 110\,\text{ps}$, $t_{OR} = 100\,\text{ps}$, $t_{NAND} = 50\,\text{ps}$? What is the minimum logic delay?

Solution:

$$t_{MAX} = 30\,\text{ps} + 80\,\text{ps} + 110\,\text{ps} + 100\,\text{ps} + 50\,\text{ps} = 370\,\text{ps}$$

$$t_{MIN} = 50\,\text{ps}$$

(b) What is the maximum clock frequency of this circuit? Are there any potential hold time violations? If there are, draw a modified circuit fixing the hold time violation. You may add or subtract gates as long as the final result remains logically equivalent, but you may not modify the clock path or clock frequency.

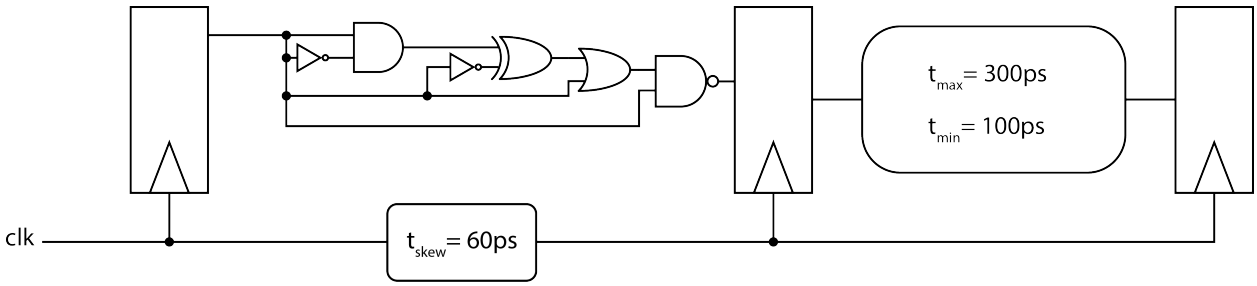
Solution:

$$f_{MAX} = (t_{MAX} + t_{clk-q} + t_{setup})^{-1} = 1.96\,\text{GHz}$$

There are no hold time violations in this circuit. If there was one, it would likely be

along the fast path that goes directly to the last NAND gate. To solve this, we could just buffer that line with inverters to increase the minimum delay and avoid a hold violation.

(c) After performing the place and route, a clock skew has been added to the second register, as pictured below.



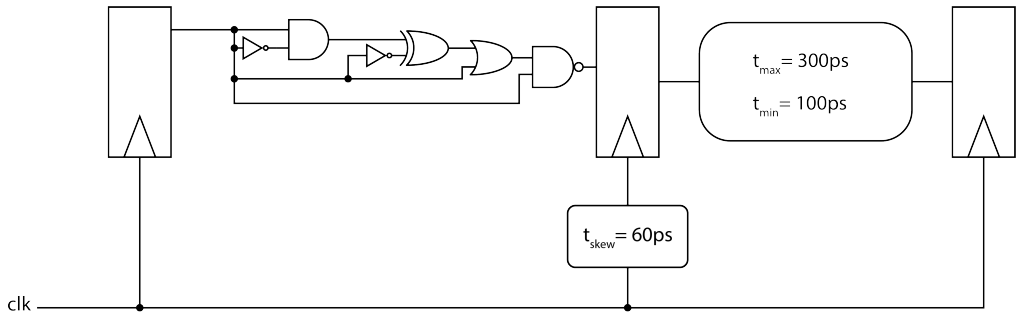
How does this affect your answers for part (a) and (b)? What is the new clock frequency? Has this now caused a hold time violation in another part of the circuit?

Solution:

The skew would allow us to run at a slightly faster frequency as the old critical path has an additional 60 ps, so the gate-level path is no longer the critical path of the overall circuit. The new critical path is now the maximum logic delay of the second combinational block, so the new max frequency is

$$f_{MAX} = (300\,\text{ps} + t_{clk-q} + t_{setup})^{-1} = 2.27\,\text{GHz}$$

If the skew had been applied as pictured below, however, the situation would be different.



The maximum frequency would still change, but now there is a setup violation in the second combinational block as there is now 60 ps *less* time from launching to receiving register, so the original clock period would be too short to accomodate even the fast logic path.

Problem 2: Error Correction Code

(a) Encode the data bitstream `10011011` with Extended (SECDED) Hamming Code

Solution:

The final output should appear as such with parity bit placeholders:

`p0 p1 p2 1 p4 0 0 1 p8 1 0 1 1`

$$p_1 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 1 = 0$$

$$p_2 = 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0 = 0$$

$$p_4 = 0 \oplus 0 \oplus 1 \oplus 1 = 0$$

$$p_8 = 1 \oplus 0 \oplus 1 \oplus 1 = 1$$

$$p_0 = 0 \oplus 0 \oplus 1 \oplus 0 \oplus 0 \oplus 0 \oplus 1 \oplus 1 \oplus 1 \oplus 0 \oplus 1 \oplus 1 = 0$$

The final sequence is thus:

`0001000111011`

(b) The following bitstreams may contain some bit errors and are encoded with Extended (SECDED) Hamming Code. If there is a single error, identify the error bit and correct the bitstream. If there is a double error, identify that there is a double bit error. Otherwise, state that there is no error.

- `1001101010010`

Solution:

Check overall parity bit:

$$p_0 = 1 = 0 \oplus 0 \oplus 1 \oplus 1 \oplus 0 \oplus 1 \oplus 0 \oplus 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0$$

Either there is no error, or there is a double-bit error. Check all other parity bits:

$$p_1 = 0 = 1 \oplus 0 \oplus 0 \oplus 0 \oplus 1$$

$$p_2 = 0 \neq 1 \oplus 1 \oplus 0 \oplus 0 \oplus 1$$

$$p_4 = 1 = 0 \oplus 1 \oplus 0 \oplus 0$$

$$p_8 = 1 = 0 \oplus 0 \oplus 1 \oplus 0$$

Parity bit 2 does not evaluate to the correct value, but the overall parity bit is correct, so there is a double bit error in this sequence.

- `0000101100101`

Solution:

Check overall parity bit:

$$p_0 = 0 \neq 0 \oplus 0 \oplus 0 \oplus 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0 \oplus 1$$

There is potentially a single-bit error. Check all other parity bits:

$$p_1 = 0 \neq 0 \oplus 0 \oplus 1 \oplus 0 \oplus 0$$

$$p_2 = 0 = 0 \oplus 0 \oplus 1 \oplus 0 \oplus 1$$

$$p_4 = 1 = 0 \oplus 1 \oplus 1 \oplus 1$$

$$p_8 = 0 = 0 \oplus 1 \oplus 0 \oplus 1$$

Parity bit 1 does not evaluate to the correct value, and none of the other parity bits evaluate to false except the overall bit. 0[0]00101100101 is the error.

- `1110100101011`

Solution:

Check overall parity bit:

$$p_0 = 1 = 1 \oplus 1 \oplus 0 \oplus 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0 \oplus 1 \oplus 0 \oplus 1 \oplus 1$$

Either there is no error, or there is a double-bit error. Check all other parity bits:

$$p_1 = 1 = 0 \oplus 0 \oplus 1 \oplus 1 \oplus 1$$

$$p_2 = 1 \neq 0 \oplus 0 \oplus 1 \oplus 0 \oplus 1$$

$$p_4 = 1 \neq 0 \oplus 0 \oplus 1 \oplus 1$$

$$p_8 = 0 \neq 1 \oplus 0 \oplus 1 \oplus 1$$

Parity bits 2,4,8 do not evaluate to the correct value, but the overall parity bit is correct, so there is a double bit error in this sequence.

Problem 3: Faults

You are a circuit designer at PineApple, Inc., which makes consumer electronics. As part of the team desigining the accelerometer chips present in every one of their myPhones, you are responsible for a rather large volume of chips all following your design. For each of the faults illustrated below, identify the type (design, manufacturing, runtime) and discuss their impact on costs for the company.

(a) One day you get a call from the lead physical design engineer, who is responsible for assembling all the parts of the accelerometer before sending the final design to the fabrication facility. She notifies you that they managed to catch a bug in the Serial Peripheral Interface handler while they were performing final verification tests.

Solution:

This is a design fault. The issue was a systematic problem in the design itself, which thankfully the design engineer caught before she sent it off to the foundry. The costs associated with this error would be the additional NRE cost incurred to fix the error,

but this should be much less than the costs needed to replace all the faulty devices had the design made it to fabrication, or worse, onto the open market.

(b) After the new myPhones have hit the market for a while, a sudden influx of customer service reports come in about the accelerometer. Curiously all of them seem to be phones that were sold within the last few months. After discussing the problem with the supply chain manager, you were able to trace all the problematic devices to a fabrication facility that recently had their photolithography machine sent in for maintenance due to some mask alignment issues.

Solution:

This is a manufacturing fault. Only the devices made with the bad lithography machine are affected by this error. The cost may be shared between the foundry and the design company depending on the terms of the contract they are under. The design company will still suffer some cost in recalling the faulty devices as well as a blow to their reputation, but the foundry may be responsible for some reparations and will also need to pay to repair the machine.

(c) You get a call from one of the retail stores where the workers there have encountered an error with the accelerometer that they can't explain. The customer came in complaining that their myPhone's accelerometer occasionally glitches, causing their phone to spontaneously change screen orientation. After asking for more details you discover that the customer in question had recently taken a round-trip trans-pacific flight to Japan.

Solution:

This is a runtime/intermittent fault. The issue is possibly caused by a particle strike that may have caused some devices to latch up, which is causing the glitchy output from the accelerometer, especially since the customer's flight across the Pacific may have exposed them and their devices to increased amounts of cosmic radiation. On face value, the costs may be just for replacing the broken device (depending on the terms of warranty), though if a device failed just from a flight, this may indicate a more serious design flaw and may require more design cycles to fix.

Problem 4: Packaging

You have just finished finalizing the design for your newest processor. Your chip is designed to operate at 1.5 GHz, and in the worst case may experience current spikes of up to 15 A at 1 V for a period of 50 ps. After finishing your chip, you send the chip specifications to a packaging company, which gives you quotes on two methods of packaging.

(a) The bond wires on offer have a series inductance of 0.5 nH/mm, and each bond wire needs to be 5 mm long to reach the chip pads. How many bond wires would you need to keep the V_{DD} supply noise spike below 10%?

Solution:

Adding more bond wires reduces the effective wire inductance.

$$L_{\text{eff}} = \frac{L_w}{n_w}$$

The largest voltage spike on the supply is therefore expressed as

$$V_{\text{spike}} = \frac{L_w}{n_w}\frac{dI}{dt} = \frac{2.5\,\text{nH}}{n_w}\frac{15\,\text{nH}}{50\,\text{ps}} = 0.1\,\text{V}$$

$$n_w = 7500$$

(b) The company also offers flip-chip solder ball attachment, which has a significantly reduced series inductance of 50 pH/mm, and are each about 1 mm long. How many solder balls would you need to achieve the same supply noise suppresion as part (a)?

Solution:

Each solder ball has the equvalent inductance of 50 bond wires in parallel

$$n_b = \frac{L_w}{L_b} = \frac{2.5\,\text{nH}}{50\,\text{pH}} = 50$$

Therefore, we will need 50 times fewer solder balls to achieve the same supply noise rejection.

$$n_b = \frac{n_w}{50} = \frac{7500}{50} = 150$$