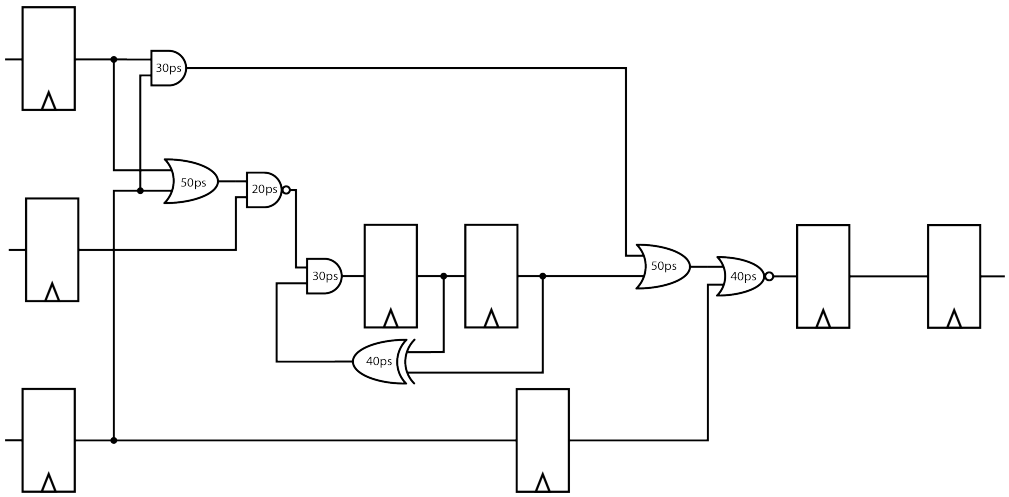
EECS 151/251A Homework 6

Due Monday, Mar 8th, 2021

Remember, please include a short (1-2 sentence) explanation with each answer unless otherwise directed in the problem.

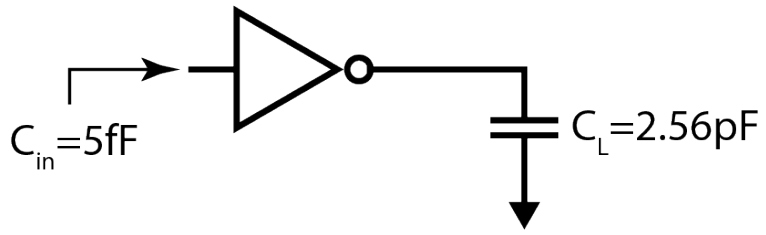
Problem 1: Retiming

Consider the circuit below. What is the critical path delay? Retime the circuit to minimize the critical path delay. What is the maximum clock frequency for the retimed circuit? The flip-flops have $t_{\text{setup}} = 20\,\text{ps}$, $t_{\text{clk-q}} = 10\,\text{ps}$, and $t_{\text{hold}} = 5\,\text{ps}$.



Problem 2: Buffer Insertion

After finishing the place-and-route process for your new ASIC design, you notice that due to a mistake in your constraint setup one of your signals is attempting to drive a very large gate directly using a minimum-sized inverter. After doing a bit of inspection of your design, you draw up the following schematic for the loading on the inverter output.



Find the optimal number of buffer stages and buffer sizes to insert between the minimum-sized inverter and the load to minimize the delay on this connection. In this technology, $\gamma = 1.5$. *You must preserve the logical function at the output as this wire carries a signal.*

Problem 3: FO4 Delay

Using the SPICE model library from previous homeworks, set up a schematic testbench to find the FO4 delay for this technology, with $W_N = W_P = 100\,\text{nm}$. Remember that this setup means an inverter driving one 4x bigger, with that inverter driving another inverter that is 4x bigger that it and measuring the delay across the inverter in the middle. Repeat with $W_N = W_P = 500\,\text{nm}$. Is the delay the same? Is this what you expect?

Problem 4: Gate Delay

Following the same steps as the gate delay calculation in the lecture, find the gate delays for the following gates. In this technology, $R_P = 2R_N$. (*HW Note: As an alternative to a short explanation at the end of your derivation, you may explain each step of your derivation as you present your work.*)

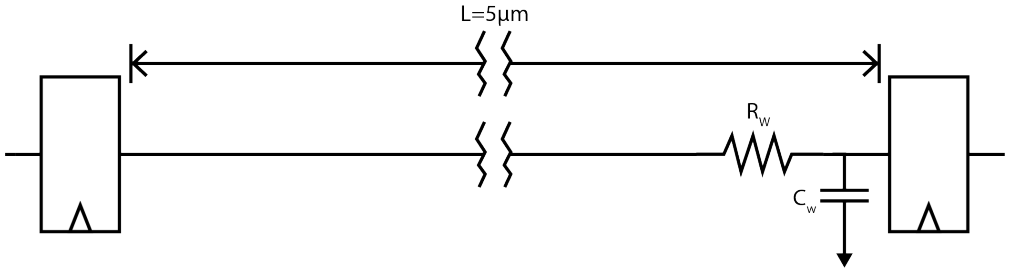
(a) 4-input NAND

(b) 3-input NOR

How would your answers change if $R_P = R_N$?

Problem 5: Wire Rebuffering

After working on your design for hours and finally putting it through the place-and-router, you're greeted with the sight you least want to see: your design failed to close timing. Heaving a heavy sigh, you open up the timing report to find that two registers on your design were placed so far away that the signal from one is not able to reach the other within a clock cycle. From the report, you are able to gather the following schematic of the connection.



In order to correct this problem, you will need to add buffers along the long wire ($r_W = 0.002\,\Omega/\mu\text{m}$, $c_W = 5 \times 10^{-3}\,\text{F/m}$) between the launching and receiving flip-flops. Find the minimum number of buffers you can add to make this path meet timing at a clock frequency of 1 GHz. You may use

any number of inverters for buffering as any inversion in the line can be made up for elsewhere. You may assume the flip-flop drives its output with the same strength and output capacitance as a minimum-sized inverter ($R_{dr} = 500\,\Omega$, $C_{int} = 2\,\text{fF}$).

Problem 6: Delays in a Physical Circuit

While performing a design review for your fellow layout engineers, you notice a long route between two identical inverters that may present a problem, illustrated below with dimensions annotated.

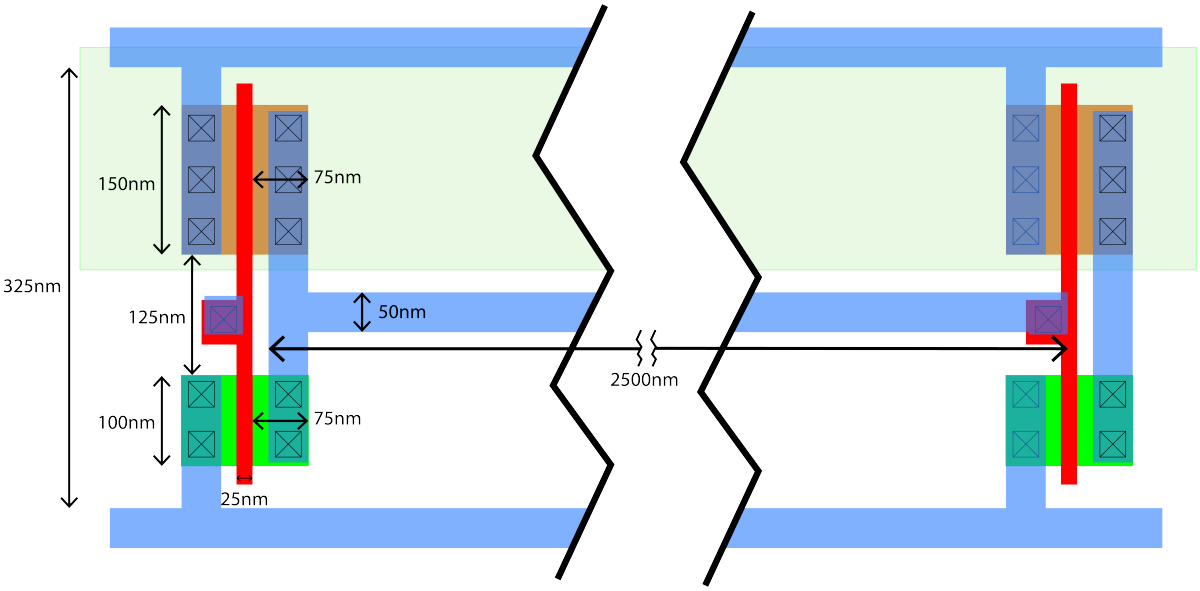


Figure 1: Layout With Annotated Dimensions

This technology has the following process parameters

Parameter	Description	Value
C_j	Bottom junction capacitance per unit area	$0.2\,\text{F/m}^2$
C_{jsw}	Sidewall perimeter capacitance per unit length	$1.6\,\text{F/nm}$
C_{ox}	Gate-bulk oxide capacitance per unit area	$0.016\,\text{F/m}^2$
$R_{\square,\text{M1}}$	Metal 1 sheet resistance	$4\,\text{m}\Omega/\square$
$R_{\square,\text{pdiff}}$	p+ diffusion sheet resistance	$0.002\,\text{m}\Omega/\square$
$R_{\square,\text{ndiff}}$	n+ diffusion sheet resistance	$0.001\,\text{m}\Omega/\square$
$R_{\square,\text{Poly}-\text{Si}}$	Polysilicon sheet resistance	$0.00001\,\text{m}\Omega/\square$
c_w	Wire parasitic capacitance per unit area	$4\,\text{mF/m}^2$
$R_{DSN,min}$	Minimum-size NMOS source-drain resistance	$700\,\Omega$ at $W = 100\,\text{nm}$
$R_{DSP,min}$	Minimum-size PMOS source-drain resistance	$1050\,\Omega$ at $W = 100\,\text{nm}$

Table 1: Process Parameters

Find the propagation delay of the first inverter given these parameters and the layout dimensions. You may assume that there is negligible parasitic contribution from the vias, source/drain metal

contacts, supply rails, and polysilicon **where it does not overlap the diffusion regions**. You must take into account the parasitic capacitances of the poly-diffusion overlap areas, however.