

EECS151/251A

Spring 2021

**Digital Design and Integrated
Circuits**

Instructors:

John Wawrzynek

Lecture 25: Faults

Announcements

- Virtual Front Row for today 4/22:
 - *Hari Vallabhaneni*
 - *Parth Nobel*
 - *Robin Chu*
 - *Jeremy Ferguson*
 - *Keyi Hu*
- **Please ask question or make comments!**
- Homework assignment 10 posted - due next Monday.
- HW 11 - final problem set - posted end of this week.

Announcements

□ End game:

14	4/20	Clock and Power Distribution		Checkpoint 2 due, , Checkpoint 3 & 4 Released	
	4/22	Testing, Faults, Error Correction Codes			
15	4/27	Inside Logic Synthesis Tools		Checkpoint 3 due	
	4/29	Wrap-up and Exam Review			
16	5/5	RRR No Lecture		Checkpoint 4	Final Checkoff due
	5/7	RRR No Lecture			
FINAL	5/14	No Class - Final Exam 7-10 PM			

Types of Faults in Digital Designs

- Design Bugs (function, timing, power draw)
 - detected and corrected at design time through testing and verification (simulation, static checks)
- Manufacturing Defects (violation of design rules, impurities in processing, statistical variations)
 - post production testing for sorting
 - spare on-chip resources for repair
- Runtime Failures (physical effects and environmental conditions)
 - assuming design is correct and no manufacturing defects

Intel Pentium FDIV Design Bug

A [hardware bug](#) affecting the [floating point unit](#) (FPU) of the [early Intel Pentium processors](#).

The processor might return incorrect binary floating point results when dividing a number. For example, the chip produced:

$$\frac{4,195,835}{3,145,727} = 1.333739068902037589$$

Instead of the correct: $\frac{4,195,835}{3,145,727} = 1.333820449136241002$

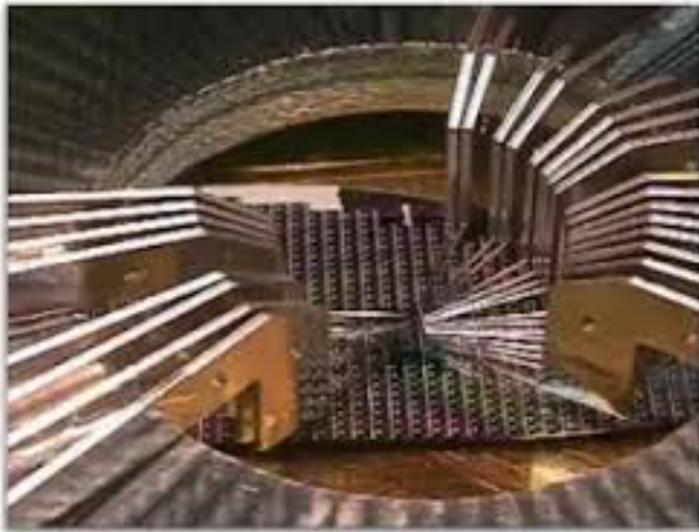
Intel attributed the error to missing entries in the lookup table used by the floating-point division circuitry.

In December 1994, Intel [recalled](#) the defective processors. In January 1995, Intel announced "a pre-tax charge of \$475 million against earnings, ostensibly the total cost associated with replacement of the flawed processors.



Dealing with Manufacturing Faults

- Designers provide “test vectors”
 - ATPG (Automatic Test Pattern Generation)
- Completed ICs are tested and “binned” for correct operation, and speed grade.



- Special circuits help speed the testing process
 - BIST (built in self test), Scan-chains

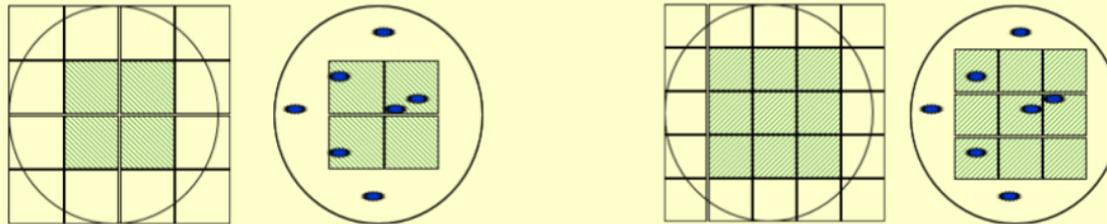
Chip Yield and Costs

- Faulty chips are discarded which effectively raises the cost of good die.

Integrated Circuits Costs

$$\text{DiesPerWafer} = \frac{\pi \times (\text{WaferDiameter}/2)^2}{\text{DieArea}} - \frac{\pi \times \text{WaferDiameter}}{\sqrt{2} \times \text{DieArea}}$$

$$\text{DieYield} = \text{WaferYield} \times \left[1 + \frac{\text{DefectsPerUnitArea} * \text{DieArea}}{\alpha} \right]^\alpha$$



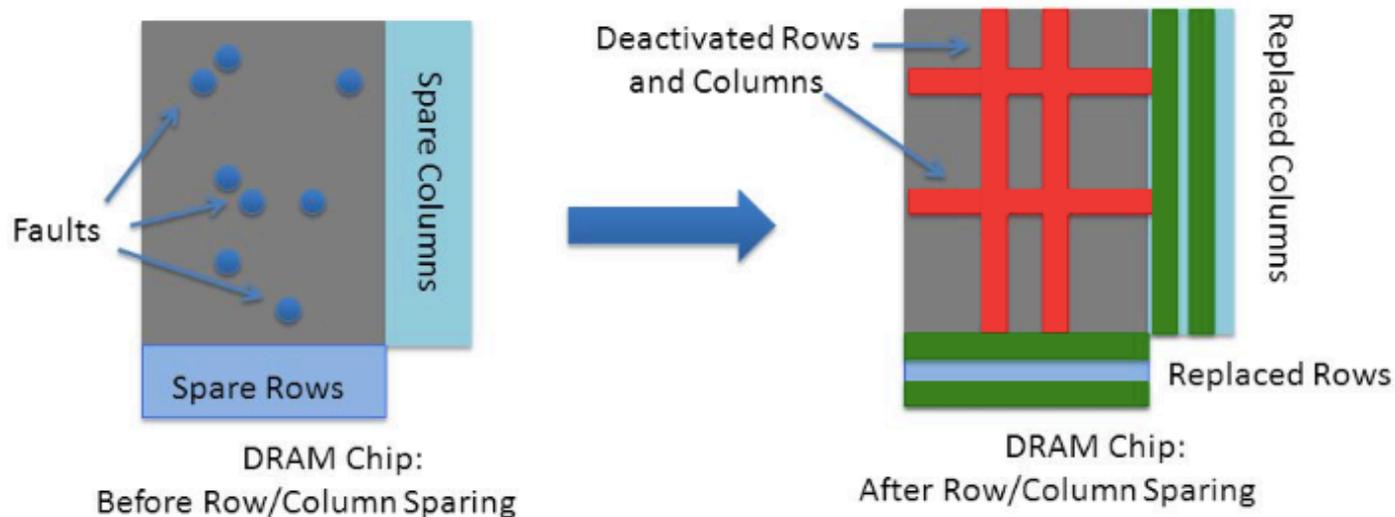
$$\text{DieCost} = \frac{\text{WaferCost}}{\text{DiesPerWafer} \times \text{DieYield}}$$

Die cost roughly goes with die area⁴

$$\text{ICCost} = \frac{\text{DieCost} + \text{TestingCost} + \text{PackingCost}}{\text{FinalTestYield}}$$

“Sparing” Helps Increase Yield

- Extra on-chip circuits wired in to replace faulty sections after manufacturing:
 - DRAM, Flash, FPGAs, multi-core processors, (mag disks)
- DRAM chip (organized into rows and columns) have spares



- Laser fuses enable spare rows/columns
- Entire row/column needs to be sacrificed for a few faulty cells

Runtime Faults

- All digital systems suffer occasional runtime faults.
 - Fault tolerant design methodologies are employed to tolerate faults in critical applications (avionics, space exploration, medical, ...)
 - Error detection and correction is commonly used in memory systems (and communication networks).
- Deeply scaled CMOS devices suffer reliability problems due to a variety of physical effects (processing, aging, environmental susceptibility)
 - Lower supply voltage for energy efficiency makes matters worse.

Physical Fault Mechanisms

- IC Runtime Faults can be classified as permanent, transient, and intermittent:
 - Permanent faults reflect irreversible physical changes (*like fused wire or shorted transistor*)
 - Transients are induced by temporary environmental conditions (*like cosmic rays and electromagnetic interference*)
 - Intermittent faults occur due to unstable or marginal hardware (*temporary ΔV_t resulting in timing error*)
- Intermittent faults often occurs repeatedly at the same location while transients affect random locations.
- Intermittent faults track changes in voltage and temperature, and may become permanent.

Physical Fault Mechanisms

- Intermittent: Aging, Voltage/Temperature Dependent
 - NBTI (negative bias temperature instability) & PBTI
 - HCI (hot carrier injection)
 - TDDB (time-dependent dielectric breakdown)
 - Electromigration

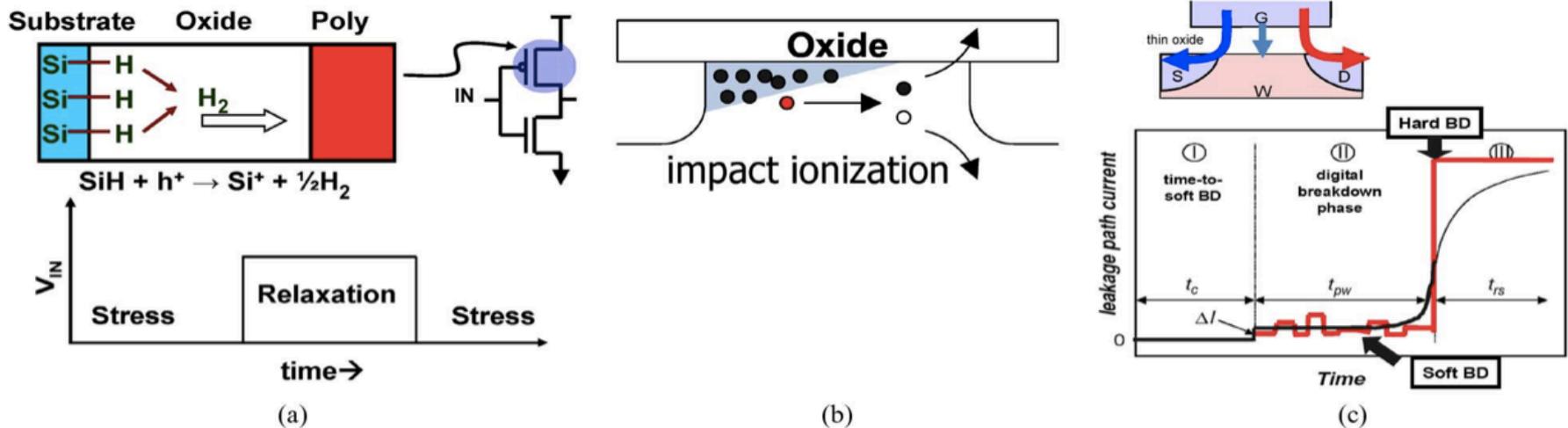


Fig. 5. Temporal variations: (a) NBTI degradation process in PMOS. Breaking of hydrogen bonds creates dangling Si that acts as a defect trap near Si-SiO₂ interface—increasing V_{TH} of the transistor. V_{TH} degradation and recovery mechanism under NBTI stress is also shown. (b) Impact ionization due to HCI. (c) Percolation path due to TDDB. The behavior of leakage current after soft and hard breakdown is also plotted.

Physical Fault Mechanisms

- NBTI, PBTI, & HCI increase V_t and decrease mobility
 - Leads to decreased performance, lower noise margins, mismatching (in SRAM), ...
- TDDB causes soft or hard gate shorts resulting in degraded transistor performance and can lead to complete transistor failure
- Electromigration reduces interconnect conductivity and can lead to open circuit.

[Ghosh and Roy: Parameter Variation Tolerance and Error Resiliency: New Design Paradigm for the Nanoscale Era, Proceedings of the IEEE | Vol. 98, No. 10, October 2010]

Transient Fault Mechanisms

Single Event Effects on digital integrated circuits: Origins and Mitigation Techniques

Dr. Raoul Velazco

TIMA Laboratory

ARIS (Reliable Architectures of Integrated Systems)

Grenoble – France

<http://tima.imag.fr>

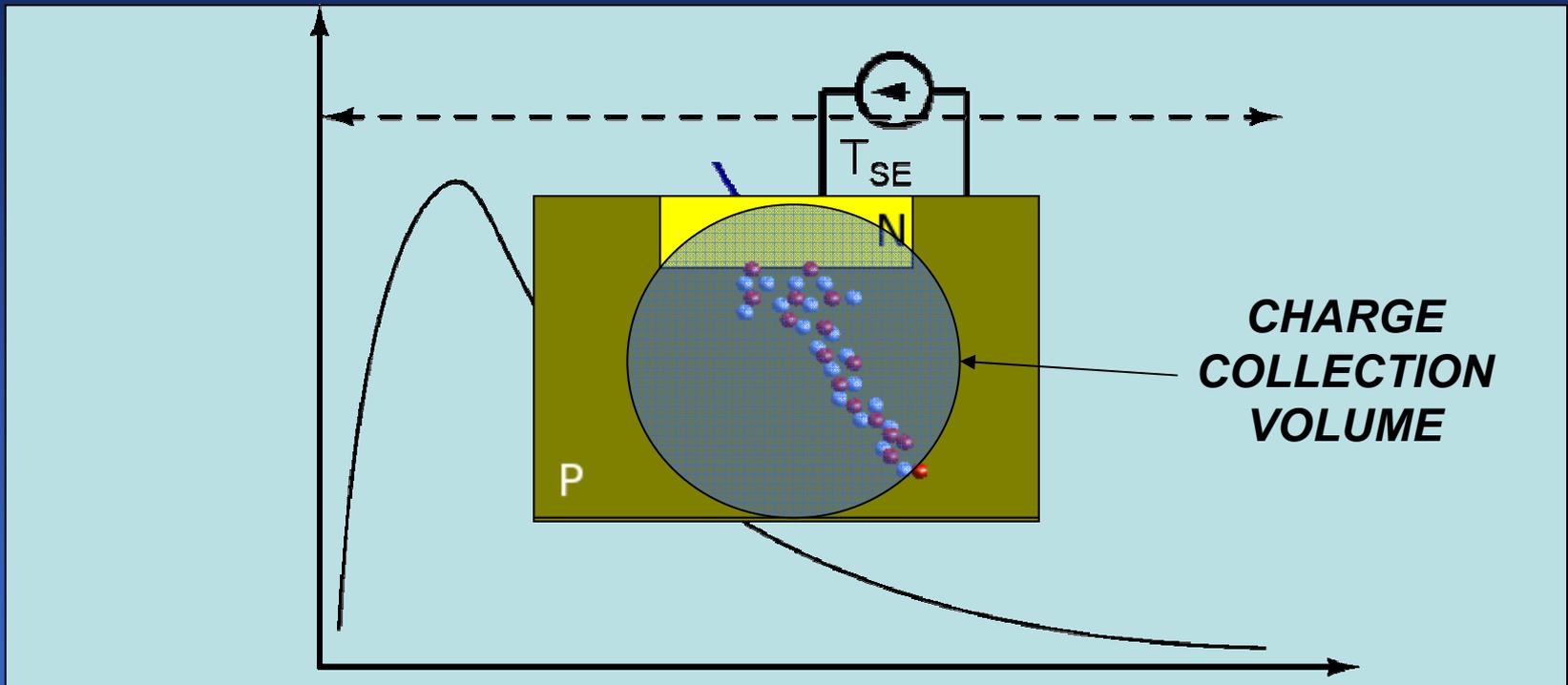
raoul.velazco@imag.fr

Ecole de Microélectronique et Microsystèmes

Fréjus, 19/5/2011

2. A Description of SEE's

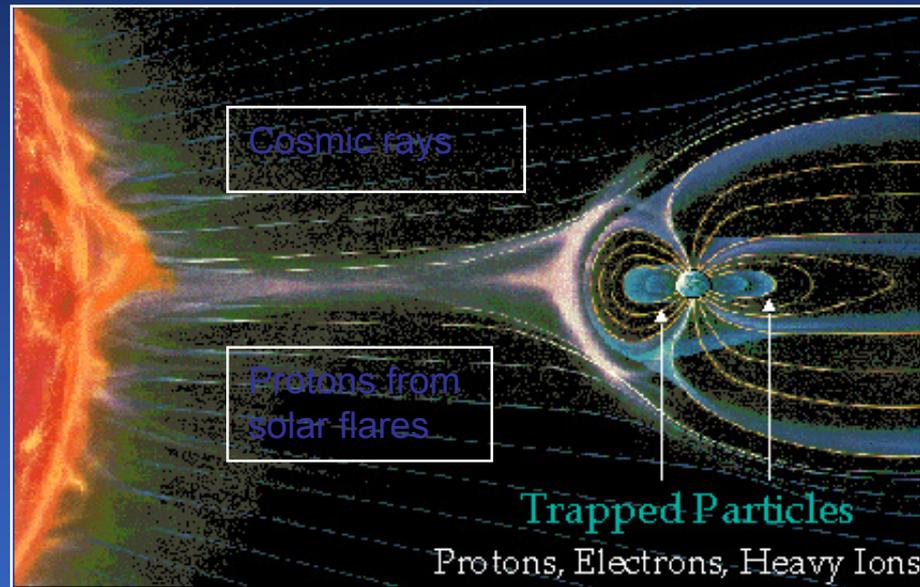
The Physical Mechanism



The incident particle generates a dense track of electron hole pairs and this ionization cause a transient current pulse if the strike occurs near a sensitive volume.

3. Sources of SEE's

Usually, SEE's have been associated with space missions because of the absence of the atmospheric shield...



Unfortunately, our quiet oasis seems to be vanishing since the enemy is knocking on the door...

- *Alpha particle from vestigial U or Th traces*
- *Atmospheric neutrons and other cosmic rays*

3. Sources of SEE's

Alpha Particles

- Sometimes, they appeared without a warning and, after some months and spending a lot of money, the source is detected*.
- In 1978, Intel had to stop a factory because water was extracted from a nearby river that, upstream, is too close to an old uranium mine.



* J. F. Ziegler and H. Puchner, "SER – History, Trends and Challenges. A guide for Designing with Memory ICs", Cypress Semiconductor, USA, 2004.

3. Sources of SEE's

Alpha Particles

- Sometimes, they appeared without a warning and, after some months and spending a lot of money, the source is detected*.
- In 1986, IBM detected a high rate of useless devices and related it to the phosphoric acid, the bottles of which were cleaned with a ^{210}P deionizer gadget...hundreds of kms far.



* J. F. Ziegler and H. Puchner, "SER – History, Trends and Challenges. A guide for Designing with Memory ICs", Cypress Semiconductor, USA, 2004.

3. Sources of SEE's

Alpha Particles

- Sometimes, they appeared without a warning and, after some months and spending a lot of money, the source is detected*.
- In 1992, the problem came from the use of bat droppings living in cavern with traces of Th and U to obtain phosphorus.

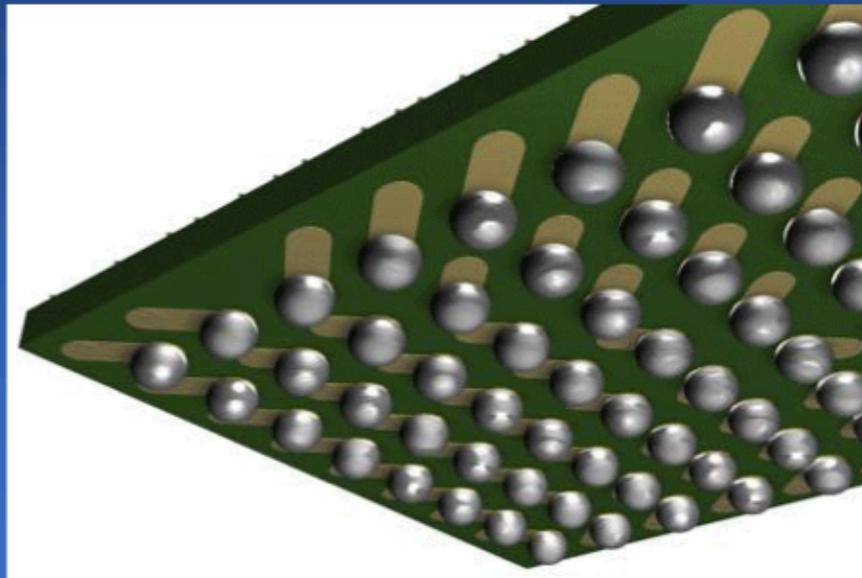


* J. F. Ziegler and H. Puchner, "SER – History, Trends and Challenges. A guide for Designing with Memory ICs", Cypress Semiconductor, USA, 2004.

3. Sources of SEE's

Alpha Particles

- But sometimes, we are a little naive...
 - Solder balls are usually made from Sn and Pb, which come from minerals where there may be uranium and thorium traces.



Nevertheless, the designer forgets this detail and places the solder balls too close to critical nodes!

3. Sources of SEE's

Cosmic Rays

Usually, they had been a headache for the designers of electronics boarded in space missions...

Here you are some of their practical jokes*...

- Cassini Mission (1997).- Some information was lost because of MBUs.
- Deep Space 1.- An SEU caused a solar panel to stop opening out.
- Mars Odyssey (2001).- Two weeks after the launch, alarms went off because some errors lately attributed to an SEU.
- GPS satellite network.- One of the satellites is out of work, probably because of a latch-up.

3. Sources of SEE's

Cosmic Rays at Ground Level

- The highest fluence is reached between 15-20 km of altitude.
- Less than 1% of this particle rain reaches the sea level.
- The composition has also changed...
 - Basically, neutrons and some pions

Usually, the neutron flux is referenced to that of New York City, its value been of (in appearance) only 15 n/cm²/h

- This value depends on the altitude (approximately, x10 each 3 km until saturation at 15-20 km).
- And also on latitude, since the nearer the Poles, the higher rate.
- South America Anomaly (SAA), close to Argentina
- 1.5 m of concrete reduces the flux to a half.

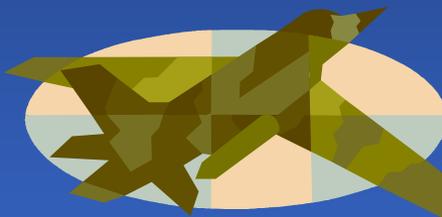
What a weak foe, really should be we afraid of?

3. Sources of SEE's

Cosmics Rays at Ground Level

Perhaps, we may believe that we are in a safe shelter but...

- 1992.- The PERFORM system, used by airplanes to manage the taking-off manoeuvre had to be suddenly replaced because of the SEUs in their SRAMs*.



- 1998.- A study reported that, every day, the 1 out of 10000 SRAMs attached to pacemakers underwent bitflips**.

This factor being 300 times higher if the patient had taken an transoceanic aircraft.

* J. Olsen, *IEEE Trans. Nucl. Sci.*, 1993, 40, 74-77

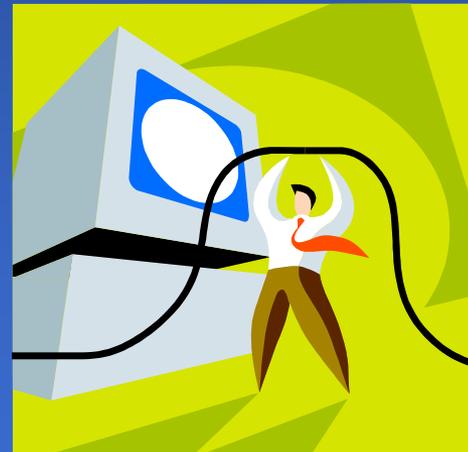
** P. D. Bradley, *IEEE Trans. Nucl. Sci.*, 45 (6), 2829-2940



3. Sources of SEE's

Cosmic Rays at Ground Level

- The call of the Thousand (2000).- Sun Unix server systems crashed in dozens of places all over the USA because of SEU's happening in their cache memory, costing several millions of dollars*.
- 2005.- After 102 days, the ASC Q Cluster supercomputer showed 7170 errors in its 81-Gb cache memory, 243 of which led to a crash of the programs or the operating system**.



* FORBES, 2000

** K. W. Harris, IEEE Trans. Dev. Mat. Reliab., 2005, 5, 336-342

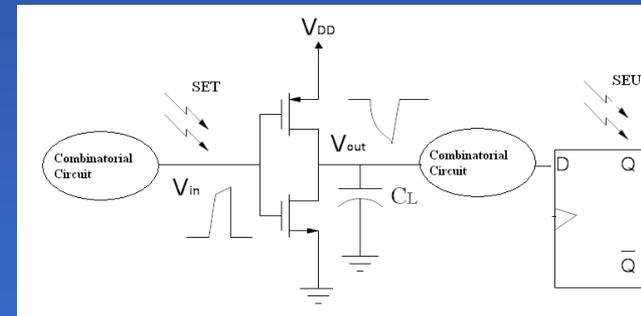
4. Mitigation of SEE's

First of all, Where must we expect SEEs?

- All the combinational stages are supposed to be affected by SETs.
- Everything having SRAM cells is a candidate to show SEUs, MBU's:
 - SRAM's, Microprocessors, FPGAs, ASICs, etc.
- Other devices seem to be quite SEE-tolerant because of their way of building:
 - DRAMs, PSRAMs, NAND memories, etc.

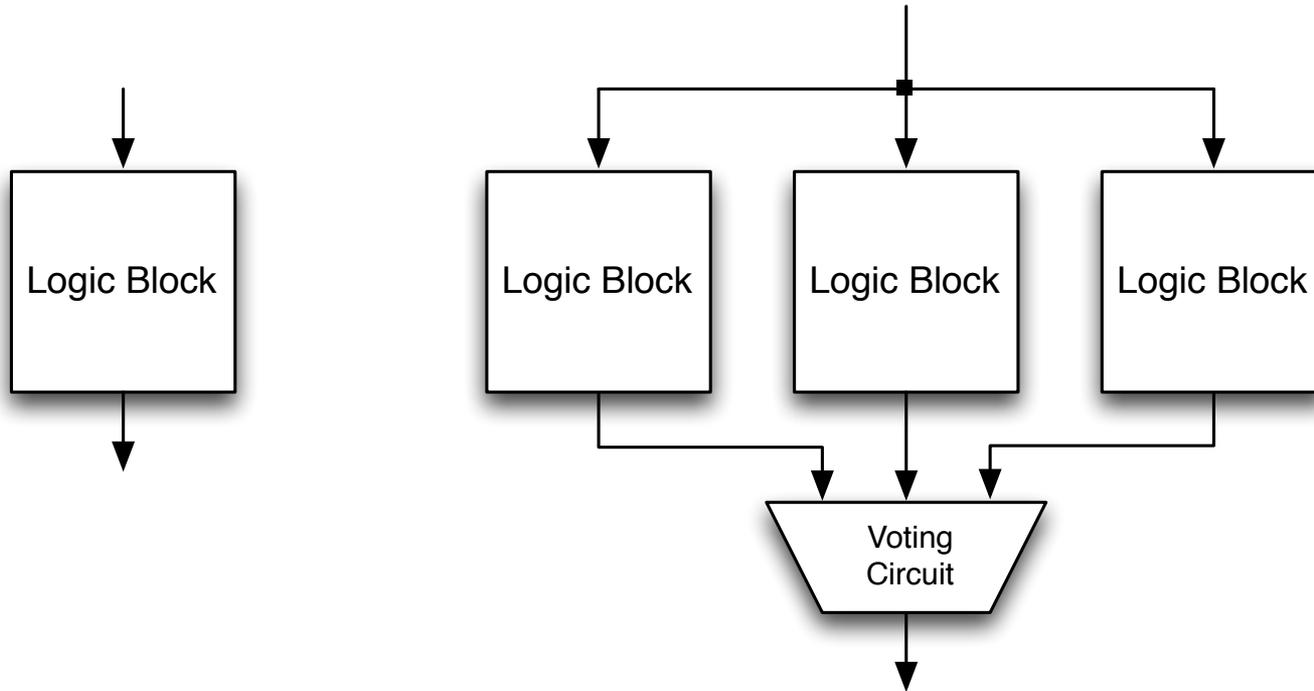
Which are the strategies to mitigate SEE's?

1. *Technological*
2. *Design*
3. *Software and Hardware Redundancy*



A Fault-Tolerant Design Methodology

- Triple-Modular Redundancy
 - relies on small / reliable voting circuit
- Most popular in space applications
-



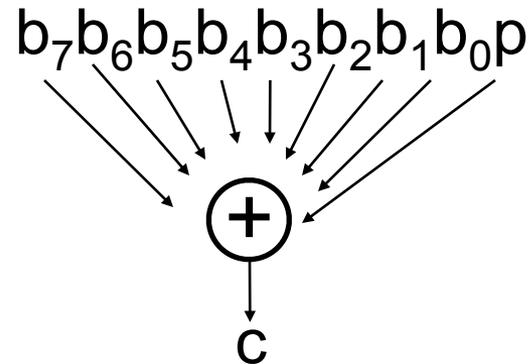
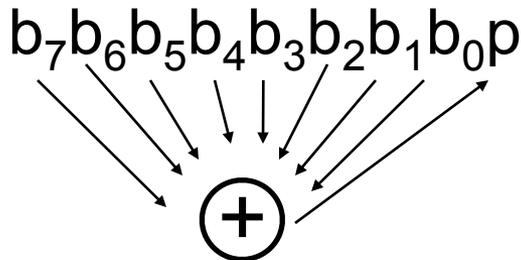
Error Correction Codes (ECC)

- Memory systems exhibit errors (accidentally flipped-bits)
 - Large concentration of sensitive nodes
 - “Soft” errors occur occasionally when cells are struck by alpha particles or other environmental upsets.
 - Less frequently, “hard” errors can occur when chips permanently fail.
- Where “perfect” memory is required
 - servers, spacecraft/military computers, ...
- Memories are protected against failures with ECCs
- Extra bits are added to each data-word
 - extra bits are used to detect and/or correct faults in the memory system
 - in general, each possible data word value is mapped to a unique “code word”. A fault changes a valid code word to an invalid one - which can be detected.

Simple Error Detection Coding

Parity Bit

- Each data value, before it is written to memory is “tagged” with an extra bit to force the stored word to have *even parity*:
- Each word, as it is read from memory is “checked” by finding its parity (including the parity bit).



- A non-zero parity indicates an error occurred:
 - two errors (on different bits) is not detected (nor any even number of errors)
 - odd numbers of errors are detected.

Hamming Error Correcting Code

- Use more parity bits to pinpoint bit(s) in error, so they can be corrected.

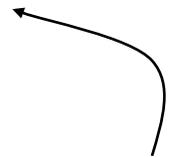
- Example: Single error correction (SEC) on 4-bit data

- use 3 parity bits, with 4-data bits results in 7-bit code word
- 3 parity bits sufficient to identify any one of 7 code word bits
- overlap the assignment of parity bits so that a single error in the 7-bit word can be corrected

- **Procedure:** group parity bits so they correspond to subsets of the 7 bits:

- p_1 protects bits 1,3,5,7
- p_2 protects bits 2,3,6,7
- p_3 protects bits 4,5,6,7

1 2 3 4 5 6 7
 p_1 p_2 d_1 p_3 d_2 d_3 d_4



Bit position number

001 = 1_{10}
 011 = 3_{10}
 101 = 5_{10}
 111 = 7_{10}

} p_1

010 = 2_{10}
 011 = 3_{10}
 110 = 6_{10}
 111 = 7_{10}

} p_2

100 = 4_{10}
 101 = 5_{10}
 110 = 6_{10}
 111 = 7_{10}

} p_3

*Note:
 number bits
 from left to
 right.*

Hamming Code Example

1 2 3 4 5 6 7

p_1 p_2 d_1 p_3 d_2 d_3 d_4

- Note: parity bits occupy power-of-two bit positions in code-word.
- On writing to memory:
 - parity bits are assigned to force even parity over their respective groups.
- On reading from memory:
 - check bits (c_3, c_2, c_1) are generated by finding the parity of the group and its parity bit. If an error occurred in a group, the corresponding check bit will be 1, if no error the check bit will be 0.
 - check bits (c_3, c_2, c_1) form the position of the bit in error.

- Example: $c = c_3c_2c_1 = 101$
 - error in 4,5,6, or 7 (by $c_3=1$)
 - error in 1,3,5, or 7 (by $c_1=1$)
 - no error in 2, 3, 6, or 7 (by $c_2=0$)
- Therefore error must be in bit 5.
- *Note the check bits point to 5*
- By our clever positioning and assignment of parity bits, the check bits always address the position of the error!
- $c=000$ indicates no error

Hamming Error Correcting Code

- Overhead involved in single error correction code:
 - let p be the total number of parity bits and d the number of data bits in a $p + d$ bit word.
 - If p error correction bits are to point to the error bit ($p + d$ cases) plus indicate that no error exists (1 case), we need:
$$2^p \geq p + d + 1,$$
thus $p \geq \log(p + d + 1)$ for large d , p approaches $\log(d)$
- Adding on extra parity bit covering the entire word can provide double error detection

1	2	3	4	5	6	7	8
p_1	p_2	d_1	p_3	d_2	d_3	d_4	p_4
- On reading the C bits are computed (as usual) plus the parity over the entire word, P :

 $C=0$ $P=0$, no error
 $C \neq 0$ $P=1$, correctable single error
 $C \neq 0$ $P=0$, a double error occurred
 $C=0$ $P=1$, an error occurred in p_4 bit

Typical modern codes in DRAM memory systems:

64-bit data blocks (8 bytes) with 72-bit code words (9 bytes),
results in SEC, DED.