Problem Set 2
Due Wednesday February 13, 2008

1. Consider a signal source modeled as a current source in parallel with a complex impedance $R+jX$. Find the optimum load impedance to maximize power transfer from the source to the load.

2. For the tuned amplifier shown below, find the transistor width for $M_1$ and $M_2$ and inductance $L$ that achieves 20 dB voltage gain at 5 GHz with minimum bias current. Assume direct voltage input drive (source impedance =0), that the Q of the inductor is 5, that transistor length=0.25\,$\mu$m and that the source and drain diffusions are 1\,$\mu$m wide*. Also you may assume that $M_1$ and $M_2$ are the same size and that both bulk nodes are grounded. How much current is required? What is the bandwidth of the amplifier? What is its output impedance at 5 GHz? Confirm your design with SPICE. Hint: find $g_m$, $r_o$ and $C_{out}$ of the composite cascode device as a function of width, calculate the inductance required to tune the amplifier to 5 GHz (as a function of width), then solve for voltage gain $A_v=V_{out}/V_{in}$.
VTO=0.4V  
KP=200µA/V²  
GAMMA=0.6  
Phi=0.6  
LAMBDA=0.15  
RD=5Ωµm  
RS=5Ωµm  
CJ* = 900 (µF/m²)  
MJ* =0.4  
PB=0.5  
CJSW* =500 (pF/m)  
MJSW* =0.4  
TOX=7nm  
CGSO=0.1 (nF/m)  
CGDO=0.1 (nF/m)

* CJ defines the unit zero voltage junction capacitance for drain and source diffusion. in F/m². MJ is the grading coefficient for these junctions. CJSW defines the sidewall junction capacitance for drain and source in F/m and MJSW the grading coefficient for that junction. In this problem we take junction area be A=W×1µm. Thus, for example,

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CBD = A \cdot \frac{CJ}{(1 - \frac{V_{BD}}{PB})MJ} + W \cdot \frac{CJSW}{(1 - \frac{V_{BD}}{PB})MJSW}
\]