A MOSFET gain stage is shown below.

\[ V_t = 0.8V \]
\[ k' = 60 \mu A/V^2 \]
\[ W/L = 10 \]

1. A MOSFET gain stage is shown below.

a) Choose \( V_{GG} \) and \( R_L \) for a bias current of 300 \( \mu A \) and a small-signal voltage gain of 3.

b) Use SPICE to plot the large signal transfer characteristic for signal input \( V_i \) between \( \pm 2V \). Verify (a).

c) Calculate \( HD_2 \) and \( HD_3 \) in \( V_o \) for a sinusoidal output voltage of 0-peak amplitude of 300 mV and also calculate the output voltage bias point shift. Verify with SPICE.

2. A power output stage is shown below.

\[ \beta_0 = 100 \]
\[ I_S = 10^{-14} A \]
\[ I_K = 400 mA \]

\[ \beta = \frac{I_C}{I_B} = \frac{\beta_0}{1 + \frac{I_C}{I_K}} \]

a) Choose \( I_X \) for a bias current \( I_{CQ} = 200 mA \).

b) Express \( I_C \) as a function of \( I_B \). Thus derive a power series linking \( (I_C - I_{CQ}) \) and \( I_B \). Thus calculate the maximum average sinusoidal signal power which can be delivered to \( R_L \) for \( HD_2 \leq 5\% \). Verify with SPICE.