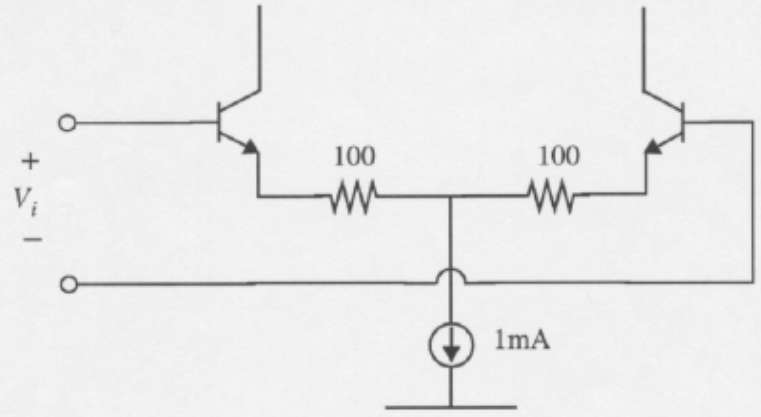
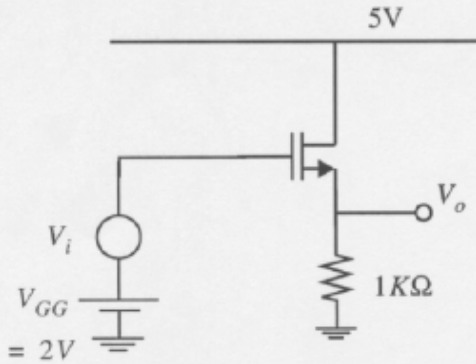
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Example Problem Set 3 **EECS 142**

1. A receiver input stage is shown below. Calculate the maximum interfering signal voltage at V_i for $IM_3 < 1\%$.



2. Calculate IM_2 and IM_3 in the circuit shown below, for two sinusoidal voltages of o-peak amplitude 300 mV each applied at V_i. Check with SPICE by simulating HD_2 and HD_3.

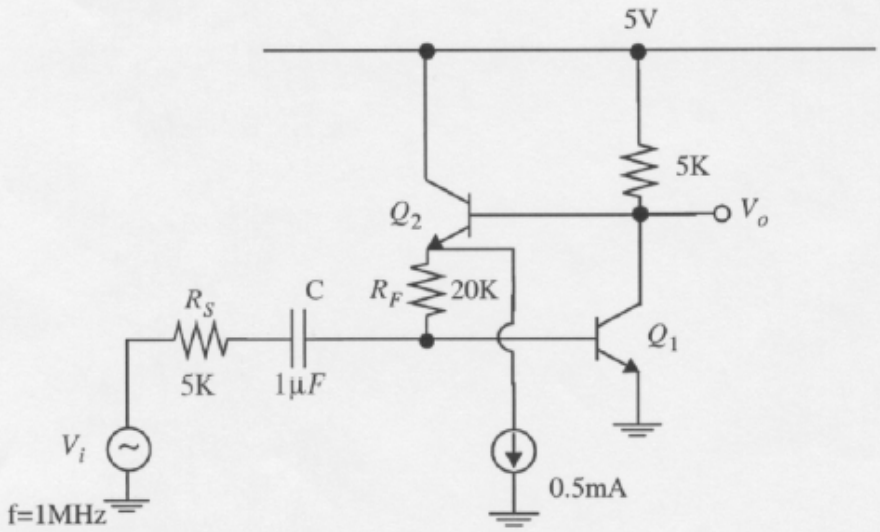


$k' = 60\mu A/v^2$

$V_t = 0.8V$

$\frac{W}{L} = 10$

3. A feedback amplifier is shown below.



$\beta_0 = 100$

$I_s = 10^{-16} A$

a) Calculate the small-signal voltage gain of the circuit and the loop gain at f = 1MHz .

b) Calculate HD_2 in V_0 for a 1V peak-peak sinusoidal output voltage at f = 1MHz , assuming Q_1 is the major source of distortion. Check with SPICE.