A wideband dc-coupled V/I converter is shown below.

\[ V_{CC} = 5V \]
Device Data

As in P.S 1 but use \( \frac{1}{4} \) size npn devices and \( \frac{1}{2} \) size pnp devices.

1. Calculate bias currents in all devices for \( V_i = 1 \text{Vdc} \).
2. Calculate and sketch the transfer function \( I_0 / V_i \) for \( V_i \) from 0 to 5V.
3. Calculate the -3dB frequency of the small-signal transfer function for \( V_i = 1 \text{Vdc} \).
4. Check the above on SPICE and also investigate and comment on temperature and supply sensitivity from -55°C to 125°C and \( V_{CC} = 4.5 - 5.5 \text{V} \).

Also use SPICE to investigate transient response for \( V_i \) steps 0.5V to 1V and 0V to 1V.

A CMOS VI converter is shown below. All PMOS wells go to +10V.

+10V

-10V

1. Calculate bias \( I_D \) and \( V_{DS} \) for all devices.
2. Calculate and sketch the \( I_0 - V_i \) transfer characteristic for \( V_i \) from -2V to +2V.
3. Use SPICE to check the above and also to determine the -3dB small-signal bandwidth of the circuit. What limits the bandwidth?
4. Using the critical field of \( E_s = 1 \text{V/}\mu \text{m} \) for velocity saturation calculate equivalent series source resistors for M1-M9 and use these in SPICE to examine the effect on the circuit transfer characteristic.
Device Data

NMOS $LD=0.1\mu m$ $V_{TO}=0.7$ $\text{GAMMA}=0.5$ $\text{PHI}=0.6$ $\text{KP}=70E-6$
LAMBDA=0.03 CGD0=0.3E-9 CGS0=0.3E-9 CJ=0.4E-3 MJ=0.5
$T0X=25E-9$ $\text{CJSW}=0.4E-9$ $\text{MJSW}=0.5$ $\text{PB}=0.6$

PMOS $LD=0.1\mu m$ $V_{TO}=0.7$ $\text{GAMMA}=0.5$ $\text{PHI}=0.6$ $\text{KP}=30E-6$
LAMBDA=0.03 CGD0=0.3E-9 CGS0=0.3E-9 CJ=0.35E-3 MJ=0.5
$T0X=25E-9$ $\text{CJSW}=0.3E-9$ $\text{MJSW}=0.5$ $\text{PB}=0.6$

PMOS WELL $CJSO(FF)=0.1 \times \text{(area bottom \(\mu m^2\)) + 1.1 \times \text{(perimeter \(\mu m\))}$

MOS dimensions

[Diagram of MOS device with dimensions labeled]

n WELL for PMOS