UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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Problem Set 5 **EECS 242**

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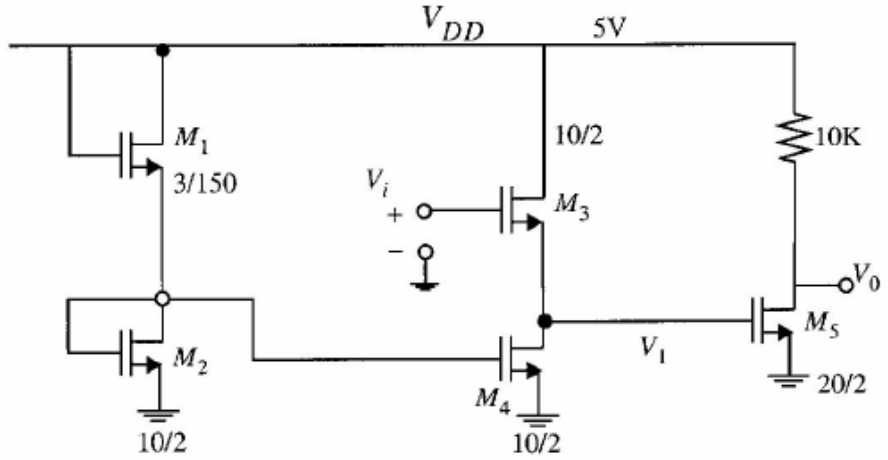
An amplifier is shown below



The dc voltage at V_i is adjusted for $V_0 = 2V$ dc.

a) Calculate bias I_D and V_{GS} for each device.

b) Calculate HD_2 and HD_3 (in dB) in V_1 and V_0 for a sinusoidal-signal voltage of 0.2V rms at V_0. Data as on P.S.5 but add $R_S = 25k\Omega/W(\mu m)$ in series with each source. Neglect charge storage and Early effect. Check using SPICE.

Hint: Start by deriving a power series for v_i as a function of v_1. Then derive v_1 as a function of v_i. Finally, cascade v_0 as a function of v_1. Neglect body effect in M_5 but not in M_3.

In the 50Ω transmission system shown below, a reverse-biased diode D is used to limit the amplitude of large negative voltage spikes on the line. However the nonlinear capacitance of the diode causes distortion in v_0. The incremental diode capacitance at the bias point is represented by

$$C = \frac{2}{\left(1 + \frac{v}{V_Q}\right)^{0.5}} pF$$

where $V_Q = 2V$ and v is the signal voltage on the diode. Capacitor C is a large coupling capacitor.

Calculate IM_2 in v_0 at $(\omega_1 - \omega_2)$ and $(\omega_1 + \omega_2)$ for two output signals in v_0 of equal amplitude 0.5V each and frequencies $f_1 = 100$ MHz and $f_2 = 101$ MHz.