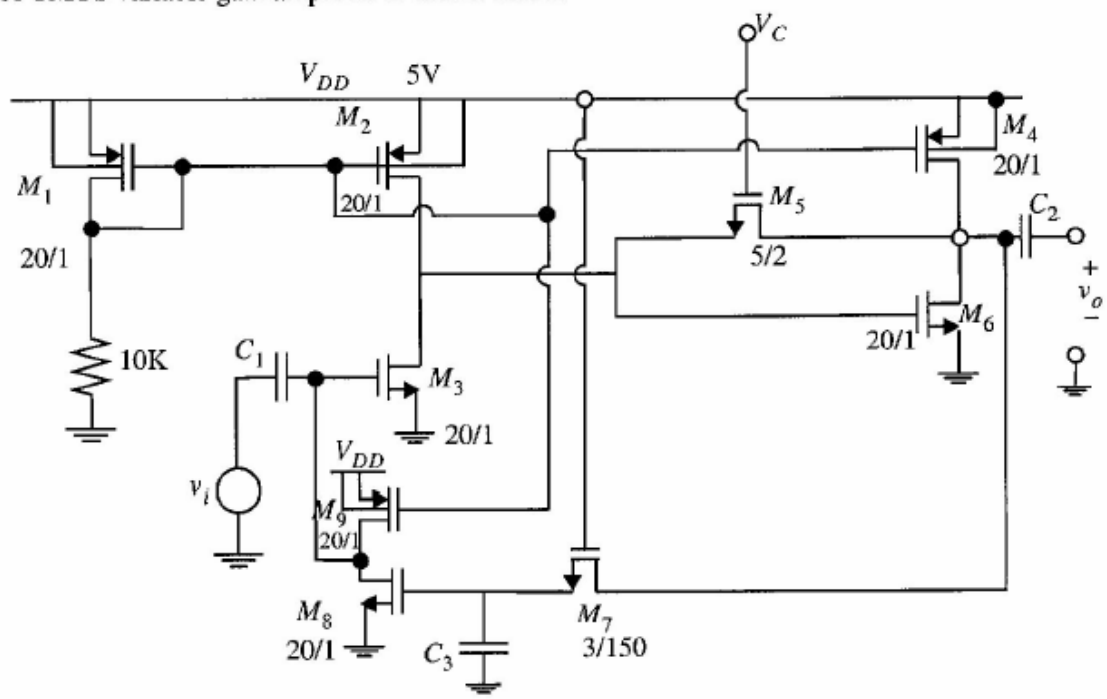
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Problem Set 7 **EECS 242**

Prof. Meyer **Spring 2006**

A CMOS variable gain amplifier is shown below.



C_1 and C_2 and C_3 are large capacitors.

1. Calculate bias current and voltage for each device.
2. Calculate the small-signal gain for dc control voltage $V_C = 3, 4, 5V$.
3. Use ZVTC to calculate the upper -3dB frequency for $V_C = 3V$. Neglect capacitance of M_7 because of its distributed structure.
4. Calculate the peak-to-peak output sinusoidal voltage swing at v_0 for $HD_2 = 10\%$ with $V_C = 3V$. Assume capacitive effects are negligible and that V_{GS5} and V_{t5} are constant.
5. Check the above on SPICE.