1) For an implementation with differentiators, we chose inductor voltages and capacitor currents as state variables

\[ I_1 = sC_1(V_2 + V_o) \]
\[ V_2 = sL_2\left(\frac{V_o}{R} + I_3\right) \]
\[ I_3 = sC_3 V_o \]

Normalize: \[ V_1 = I_1 \cdot R \quad V_3 = I_3 \cdot R \quad C_2 = \frac{L_2}{R^2} \]

\[ V_1 = sRC_1(V_2 + V_o) \]
\[ V_2 = sRC_2(V_o + V_3) \quad \text{(Note that } V_o \text{ is not the same as } V_3...) \]
\[ V_3 = sRC_3 V_o \]

Where is the input?? Use KVL, KCL to get:

\[ V_o = \frac{1}{2} \left(V_i - V_1 - V_2 - V_3\right) \]

Circuit Diagram:

(Looks quite interesting...)
After gain scaling:
2) Worst case alias frequency:  
\[ f_a = f_s - 1\text{MHz} \]

For greater 60dB attenuation:
(One frequency decade)
\[ f_a > 10 \cdot 1\text{MHz} \]
\[ f_s - 1\text{MHz} > 10\text{MHz} \]
\[ f_s > 11\text{MHz} \]

3) 
\[ f_{out} = 1.25f_s - f_s \]
\[ f_{out} = 0.25f_s \]

\[ H(s) = \frac{RC_s}{1 + 2RC_s} \]
\[ A_{out} = A \left| H(j2\pi f_{out}) \right| \]
\[ A_{out} = A \cdot \frac{RC \cdot 2\pi f_{out}}{\sqrt{1 + \left(2RC \cdot 2\pi f_{out}\right)^2}} \]

4) Every other code missing - this is the same as a 9-bit ADC, so
\[ \text{SNR} := 6.02 \cdot 9 + 1.76 \quad \boxed{\text{SNR} = 55.94} \text{[dB]} \]

5) Phase1:  
\[ Q = V_1(C_a + C_b) \]
Phase2:  
\[ Q = V_o \cdot C_a + V_2 C_b \]
\[ Q = V_1(C_a + C_b) \left| \text{substitute, } Q = V_o \cdot C_a + V_2 C_b \rightarrow \left( -V_2 C_b + V_1 C_a + V_1 C_b \right) \right| \]
\[ \text{solve, } V_o \]
\[ V_o(z) = V_1 \left( 1 + \frac{C_b}{C_a} \right) \left( \frac{1}{2} - V_2 \frac{C_b}{C_a} \right) \]