Sampling

Ideal Sampling

Practical Sampling

• Grab exact value of $V_{in}$ when switch opens

• $kT/C$ noise
• Finite $R_{sw} \rightarrow$ limited bandwidth
• $R_{sw} = f(V_{in}) \rightarrow$ distortion
• Switch charge injection (EE240)
• Clock jitter

$kT/C$ Noise

$$\frac{k_BT}{C} \leq \frac{\Delta^2}{12}$$

$$C \geq 12k_BT \left(\frac{2^B - 1}{V_{FS}}\right)^2$$

In high resolution ADCs $kT/C$ noise usually dominates overall error (power dissipation argument).

<table>
<thead>
<tr>
<th>$B$</th>
<th>$C_{min}$ ($V_{FS} = 1V$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
</tr>
<tr>
<td>14</td>
<td>13 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
</tr>
</tbody>
</table>
Acquisition Bandwidth

- The resistance $R$ of switch $S_1$ turns the sampling network into a lowpass filter with risetime $= RC = \tau$

- Assuming $V_{in}$ is constant during the sampling period and $C$ is initially discharged (a good idea—why?):

$$v_{out}(t) = v_{in}(1 - e^{-t/\tau})$$

Switch On-Resistance

- Example:

$$R = \frac{1}{2f_s C \ln(2^n - 1)}$$

$$V_{in} = V_{fs}$$

$$\frac{T}{\tau} >> 19.4, \quad R << 40\Omega$$

$$B = 14, \quad C = 13\text{pF}, \quad f_s = 100\text{MHz}$$
Switch On-Resistance

\[ I_{D\text{dimon}} = \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{in}}{2} \right) V_{DS} \]

\[ \frac{1}{R_{ON}} = \left. \frac{dI_{D\text{dimon}}}{dV_{DS}} \right|_{V_{in}=0} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \]

\[ = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{TH} - V_{in})} \]

\[ = \frac{1}{R_s \left( 1 - \frac{V_{in}}{V_{DD} - V_{TH}} \right)} \quad \text{with} \quad R_s = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{TH})} \]

\[ R_{ON} = R_s \left( 1 - \frac{V_{in}}{V_{DD} - V_{TH}} \right) \]

Sampling Distortion

\[ V_{out} = V_{in} \left( 1 - e^{-\frac{T}{2\tau}} \right) \]

\[ V_{DD} - V_{TH} = 2V \quad V_{FS} = 1V \]

\[ T/\tau = 10 \]

\[ N = 1024 \quad SNR = 61.9 \text{dB} \quad SDR = 49.2 \text{dB} \quad SNDR = 47.4 \text{dB} \quad SFDR = 49.3 \text{dB} \]
Sampling Distortion

- SFDR is very sensitive to sampling distortion
- Solutions:
  - Overdesign switches → increased switch charge injection
  - Complementary switch
  - Maximize $V_{DD}/V_{FS}$ → increased noise
  - Constant $V_{GS}$? $f(V_{in})$ → ...

$T/\tau = 20$
$V_{DD} - V_{TH} = 2V$
$V_{FS} = 1V$

Constant $V_{GS}$ Sampling

- Switch overdrive voltage is independent of signal
- Error from finite $R_{ON}$ is linear (to first order)
Constant $V_{GS}$ Sampling

boosted clock

$V_G$  
$V_{dd}$  
$V_i$  
input signal

Constant $V_{GS}$ Sampling Circuit
Clock Multiplier

Constant $V_{gs}$ Sampler: $\Phi$ LOW

- Sampling switch M11 is OFF
- C3 charged to VDD
Constant $V_{GS}$ Sampler: $\Phi$ HIGH

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant $V_{GS} = VDD$

Constant $V_{GS}$ Sampling

- Graph showing waveforms with constant $V_{GS}$ sampling.
Complete Circuit


CMOS Sample & Hold
CMOS Sample & Hold

• S1 is an n-channel MOSFET
• S1 provides as much of the sampling path resistance as possible ($R = R_{S1A} + R_{S1}$)
  – S1A is a wide (much lower resistance than S1) constant $V_{GS}$ switch
  – If S1A’s resistance is negligible, aperture delay depends only on S1 resistance
  – S1 resistance is independent of $v_{IN}$; hence, aperture delay is independent of $v_{IN}$
Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C
  - This unwanted charge is called “charge injection”
- The circuit on slide 15.2 has charge injection that varies in a wildly nonlinear fashion with $v_{IN}$
- With the CMOS Sampling Circuit, charge injection comes only from S1 and is first-order independent of $v_{IN}$
  - Only a dc offset is added to the input signal
  - This dc offset can be removed with a differential architecture

CMOS Sample & Hold

- Only 1 transistor in S1 opens to sample the input
CMOS Sample & Hold

- During $\phi_2$, the opamp buffers the sampling capacitor for loads that need it.
- The hold topology is shown on the following slide...
Jitter

- All of the preceding analyses assume that sampling impulses are spaced evenly in time
- In the real world, separation of sampling impulses has some distribution around the nominal value $T$
- The variability in $T$ is called jitter

Jitter

- The dominant cause of clock jitter in most chips is power supply noise produced by unrelated activity in other parts of the chip
- The inverter symbol represents a chain of gates in the sampling clock path
Jitter

- Let’s assume the inverter delay is 100 psec, and that the delay varies by 20% per volt change in VDD (20 psec/V)
- 200 mV of power supply noise becomes 4 psec of clock jitter

Jitter

- Sampling jitter adds an error voltage proportional to the product of (t_J - t_0) and the derivative of the input signal at the sampling instant
- Jitter doesn’t matter when sampling dc signals
Jitter

• The error voltage is

\[ e = x'(t_0)(t_J - t_0) \]

Jitter Example

Sinusoidal input

- Amplitude: \( A \)
- Frequency: \( f_s \)
- Jitter: \( \Delta t \)

\[ x(t) = A \sin(2\pi f_s t) \]
\[ x'(t) = 2\pi f_s A \cos(2\pi f_s t) \]
\[ |x'(t)| \leq 2\pi A \]
\[ |e(t)| \leq |x'(t)|\Delta t \]

Worst case

- \( A = A_{FS} \)
- \( f_s = f_s/2 \)
- \( |e(t)| \ll \frac{\Delta}{2} \equiv \frac{A_{FS}}{2^{B+1}} \)
- \( \Delta t \ll \frac{1}{2^B \pi f_s} \)

<table>
<thead>
<tr>
<th>( B )</th>
<th>( f_s )</th>
<th>( \Delta t )</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>10 MHz</td>
<td>0.5 ps</td>
</tr>
<tr>
<td>12</td>
<td>100 MHz</td>
<td>0.8 ps</td>
</tr>
<tr>
<td>8</td>
<td>1000 MHz</td>
<td>1.2 ps</td>
</tr>
</tbody>
</table>
The Jitter Law

- The worst case looks pretty stringent … what about the “average”?
- Let’s calculate the mean squared jitter error (variance)
- If we’re sampling a sinusoidal signal
  \[ x(t) = A \sin(2\pi f_x t), \]
  then
  - \[ x'(t) = 2\pi f_x A \cos(2\pi f_x t) \]
  - \[ E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2 \]
- If jitter is uniformly distributed from \(-\tau/2\) to \(+\tau/2\)
  - \[ E\{(t_J - t_0)^2\} = \tau^2/12 \]

- If \( x'(t) \) and the jitter are independent
  - \[ E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\} E\{(t_J - t_0)^2\} \]

- Hence, the jitter error power is
  \[ E\{e^2\} = \pi^2 f_x^2 A^2 \tau^2/6 \]

- If the jitter is uncorrelated from sample to sample, this “jitter noise” is white
The Jitter Law

\[ DR_{jitter} = \frac{A^2/2}{\pi^2 f_x^2 A^2 \tau^2 / 6} \]

\[ = \frac{3}{\pi^2 f_x^2 \tau^2} \]

\[ = -20 \log_{10}(f_x \tau) - 5.172 \text{dB} \]

<table>
<thead>
<tr>
<th>( f_x )</th>
<th>( \tau )</th>
<th>DR(_{\text{max}})</th>
<th>ENOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>1 ns</td>
<td>55 dB</td>
<td>8.8</td>
</tr>
<tr>
<td>1 MHz</td>
<td>2 ps</td>
<td>109 dB</td>
<td>17.8</td>
</tr>
<tr>
<td>100 MHz</td>
<td>0.4 ps</td>
<td>83 dB</td>
<td>13.5</td>
</tr>
<tr>
<td>1000 MHz</td>
<td>0.5 ps</td>
<td>61 dB</td>
<td>9.8</td>
</tr>
</tbody>
</table>

The Jitter Law

- The Jitter Law must be respected whenever you require high-resolution conversion of high frequency signals
  - Sampling a 1MHz signal with 1nsec of peak-to-peak jitter yields a dynamic range of only 55dB

- In practice, jitter is usually controlled to add negligible to the total converter error (i.e. thermal and quantization noise)

- This translates into the jitter being ~10dB below other noise sources
  - For 16 Bit conversion of 1MHz signals, a ~109dB jitter DR limit requires < 2 psec peak-to-peak jitter
The Jitter Law

- Clock jitter in the single-digit picosecond range doesn’t just happen
  - Separate supplies
  - Separate analog and digital clocks
  - Short inverter chains between clock and sampling switch
- Few, if any, other analog-to-digital conversion nonidealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input frequency
  - RMS noise proportional to input amplitude
- So, if sampling clock jitter is limiting your dynamic range, it’s easy to tell, but difficult to fix
  - Very difficult to fix in silicon without all-layer mask revisions