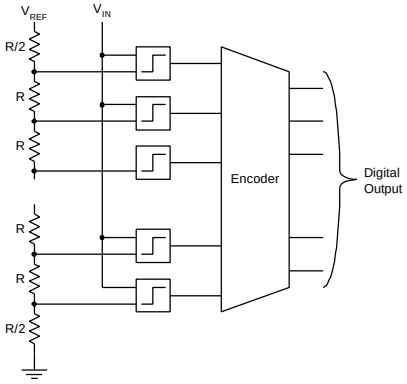
High-Speed A/D Converter

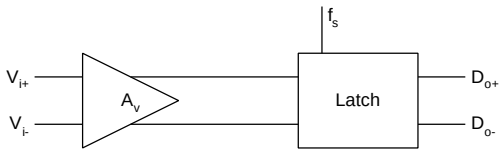
- Flash Converter
  - Comparator
  - Binary Encoder
- Interpolation
- Folding

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance

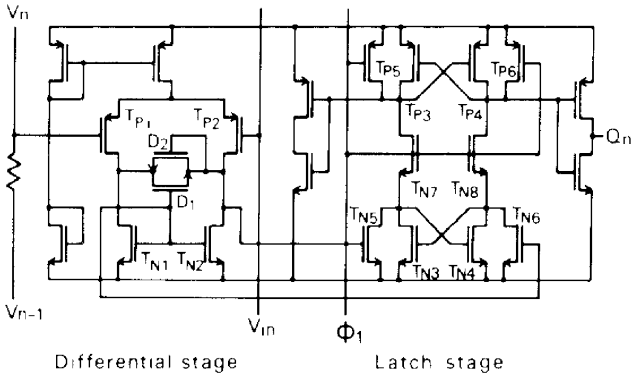


Comparator



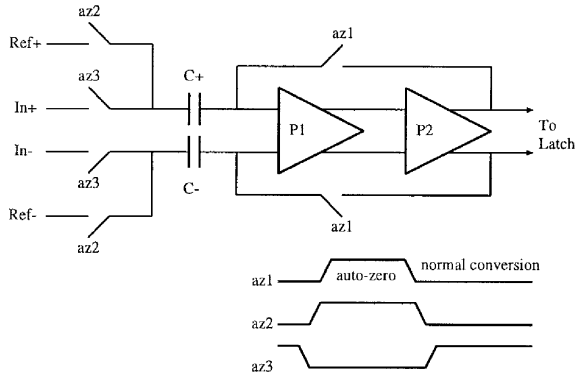
- Clock rate f_s
- Resolution
- Overload Recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

CMOS Comparator Example



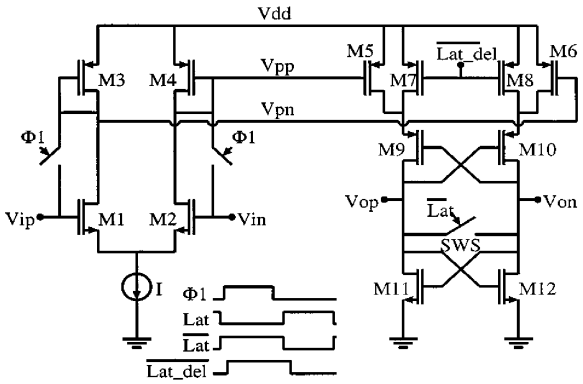
A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," JSSC June 1985, pp. 775-9.

Comparator with Auto-Zero



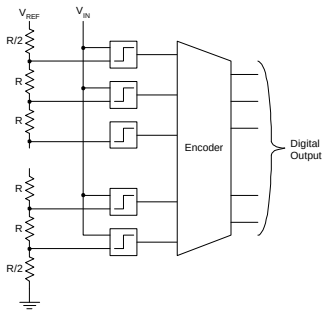
I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Auto-Zero Implementation



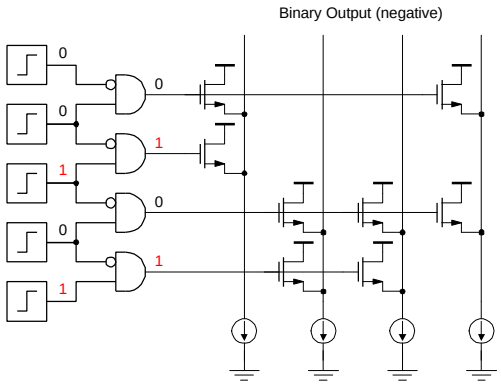
I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," JSSC March 2000, pp. 318-25.

Flash Converter Errors



- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

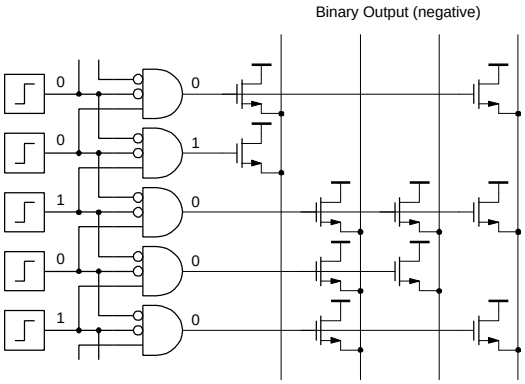
Sparkle Codes



Correct Output:
0110 … 1000

Actual Output:
1110

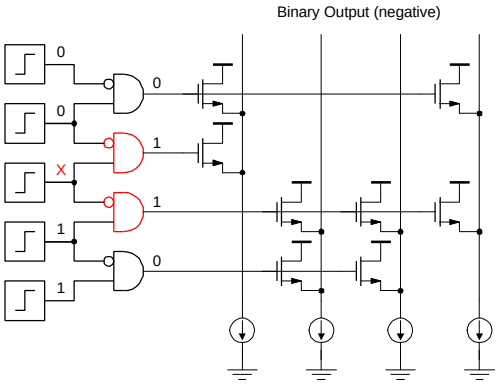
Sparkle Tolerant Encoder



Protects against a *single* sparkle.

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002.

Meta Stability



Different gates interpret metastable output X differently

Correct Output: 0111 or 1000

Actual Output: 1111

Solutions:
- Latches (high power)
- Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40.

Gray Encoding

Thermometer Code							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

Reducing Complexity

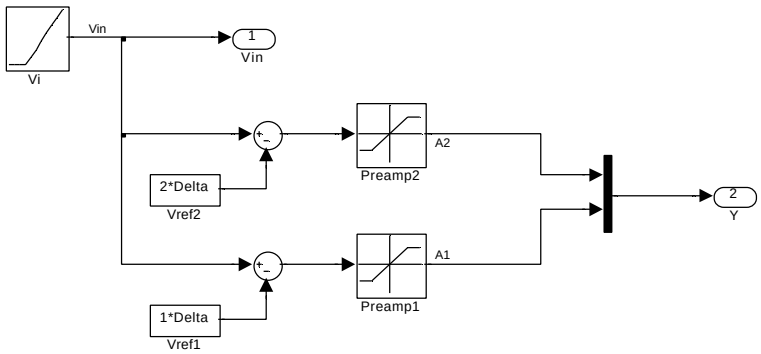
E.g. 10-bit “straight” flash
- Input range: 0 … 1V
- LSB = Δ: ~ 1mV
- Comparators: 1023 with offset << LSB
- Input capacitance: 1023 * 100fF = 102pF
- Power: 1023 * 3mW = 3W

Techniques:
- Interpolation
- Folding
- Folding & Interpolation
- Two-step, pipelining

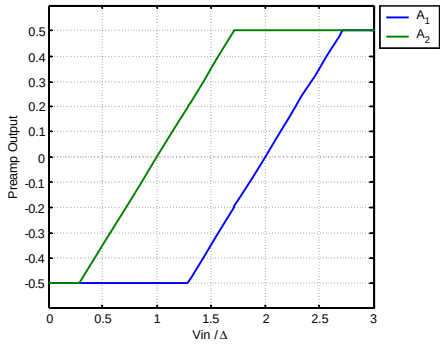
Interpolation

- Idea
  - Interpolation between preamp outputs
- Reduces number of preamps
  - Reduced input capacitance
  - Reduced area, power dissipation
- Same number of latches
- Important “side-benefit”
  - Decreased sensitivity to preamp offset
  - → improved DNL

Simulink Model



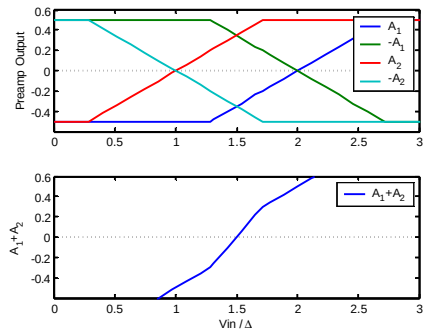
Preamp Output



Zero crossings (to be detected by latches) at V_{in} =

$V_{ref1} = 1\ \Delta$
$V_{ref2} = 2\ \Delta$

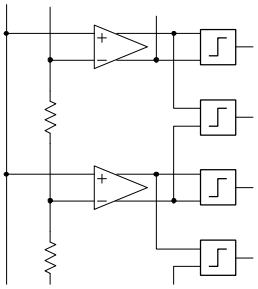
Differential Preamp Output



Zero crossings at V_{in} =

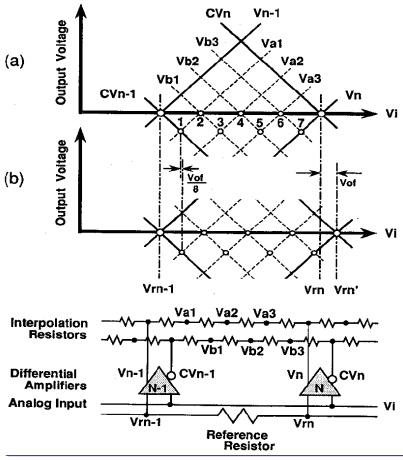
$V_{ref1} = 1\ \Delta$
$V_{ref12} = 0.5*(1+2)\ \Delta$
$V_{ref2} = 2\ \Delta$

Interpolation in Flash ADC



Half as many reference voltages and preamps

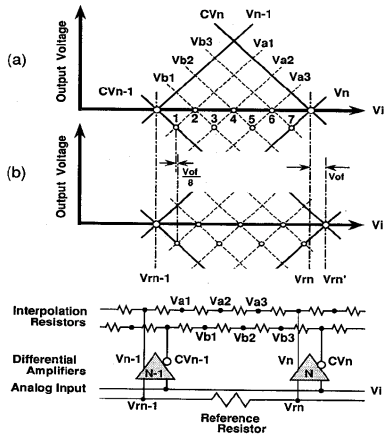
Resistive Interpolation



- Resistors produce additional levels
- With 4 resistors, the "interpolation factor" M=8 (ratio of latches/pramps)

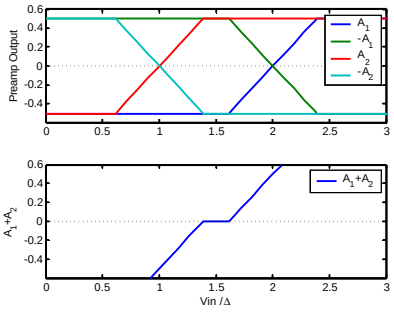
Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Convterter," JSSC April 1993, pp. 438-446.

DNL Improvement



- Preamp offset distributed over M resistively interpolated voltages:
  → impact on DNL divided by M
- Latch offset divided by gain of preamp
  → use "large" preamp gain …

Preamp Input Range



Linear preamp input ranges must overlap
i.e. range > Δ

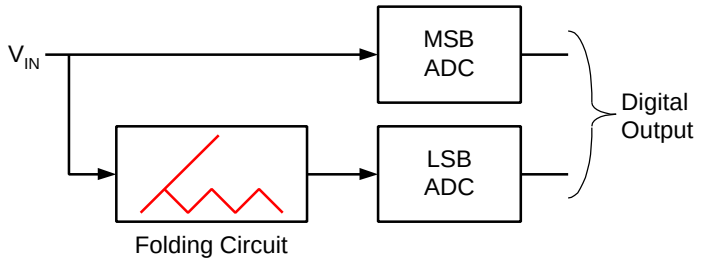
Sets upper bound on gain
<< V_{DD} / Δ

Measured Performance

Resolution		**10 b**
Maximum conversion frequency		**300 MHz**
Integral non-linearity		**±1.0 LSB**
Differential non-linearity		**±0.4 LSB**
SNR/THD	**10MHz input**	**56/-59 dB**
	50MHz input	**48/-47 dB**
Input capacitance		**8 pF**
Input range		**2 V**
Power supply		**-5.2V**
Power dissipation		**4.0W**
Chip size		**9.0 × 4.2 mm²**
Element count		**36,000**
Technology		**1.0 μm bipolar:ft=25GHz**

Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Convterter," JSSC April 1993, pp. 438-446.

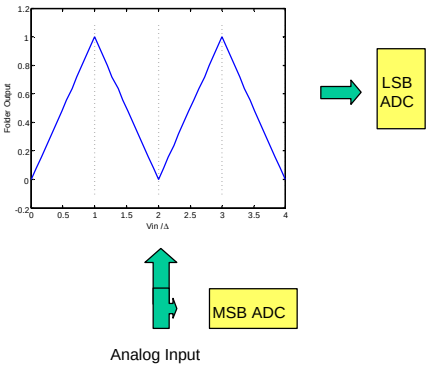
Folding Converter



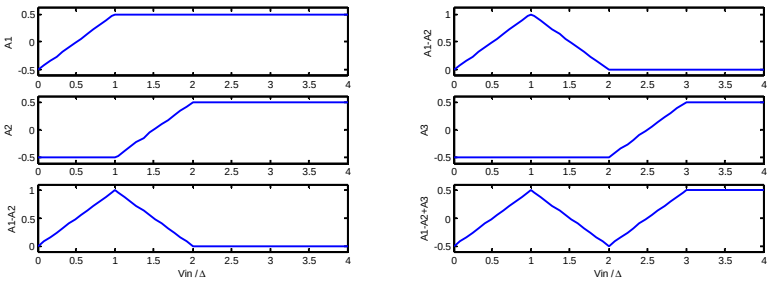
- Significantly fewer comparators than flash ~$2^{B/2+1}$
- Fast
- Nonidealities in folder limit resolution to ~10Bits

Folding

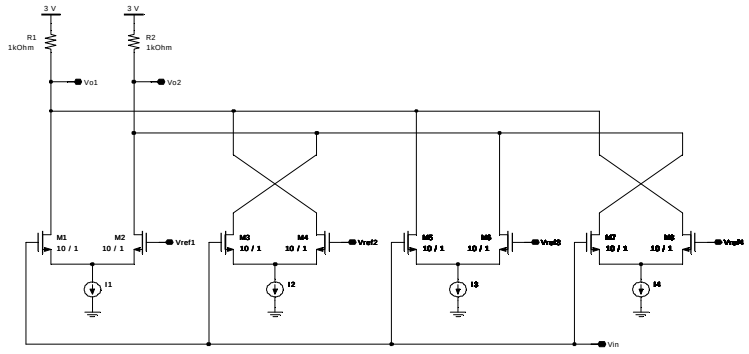
- Folder maps input to smaller range
- MSB ADC determines which fold input is in
- LSB ADC determines position within fold
- Logic circuit combines LSB and MSB results



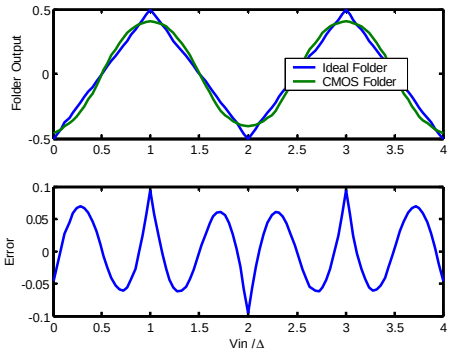
Generating Folds



Folding Circuit



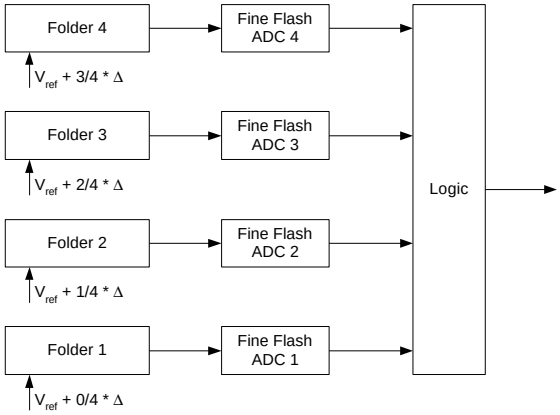
CMOS Folder Output



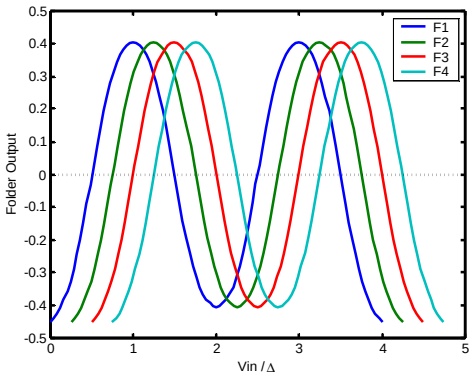
Accurate only at zero-crossings

Lowdown →
Most folding ADCs do not actually use the folds, but only the zero-crossings!

Parallel Folders



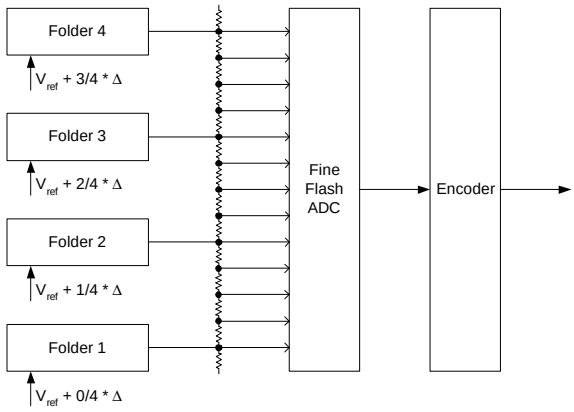
Parallel Folder Outputs



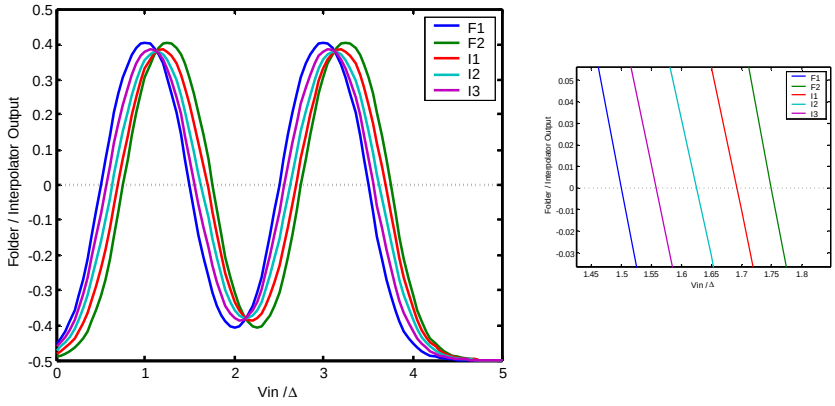
- 4 Folders
- 8 Zero crossings
- → only 3 LSB bits

- Better resolution
  - More folders
    → huge complexity
  - Interpolation

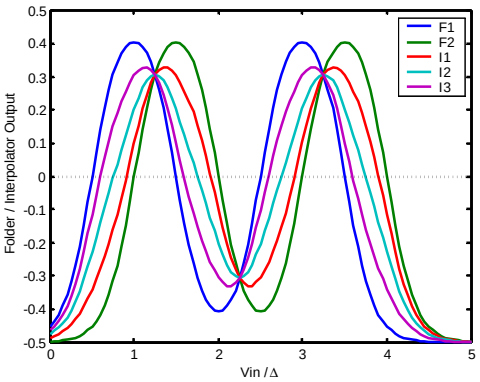
Folding & Interpolation

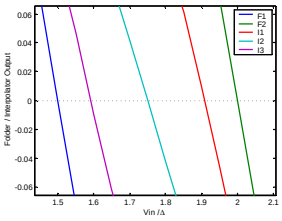


Folder / Interpolator Output



Folder / Interpolator Output

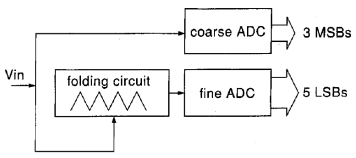


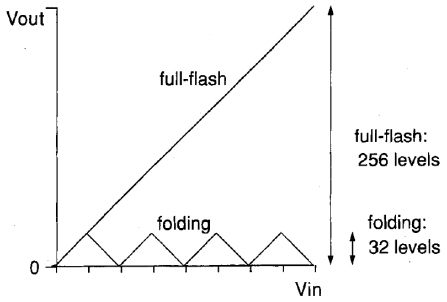


Interpolate only between closely spaced folds to avoid nonlinear distortion

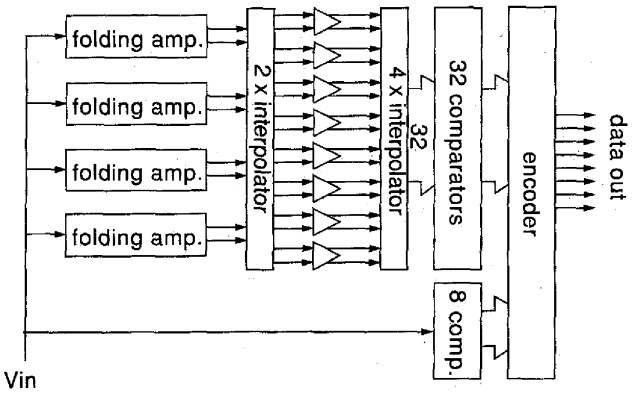
A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter

B. Nauta and G. Venes, JSSC Dec 1985, pp. 1302-8

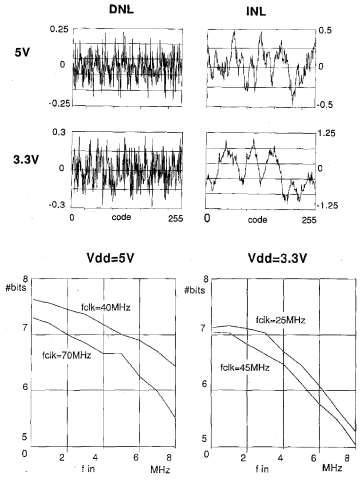




A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter



A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter



parameter		
resolution	8bit	
input capacitance	4.8 pF	
reference ladder resistance	720 Ω	
active area	0.7 mm^2	
technology	0.8μm, 1 poly , 2 metal, CMOS	
supply voltage	V_{dd}=5V	V_{dd}=3.3V
analog input	2Vpp	1.4Vpp
Integral nonlinearity	$\pm 0.5LSB$	$\pm 1.0LSB$
Differential nonlinearity	$\pm 0.2LSB$	$\pm 0.3LSB$
max. clock frequency	70MHz	45MHz
power dissipation	110mW	45mW