High-Speed A/D Converter

- Flash Converter
  - Comparator
  - Binary Encoder
- Interpolation
- Folding

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: $2^n-1$ comparators
- High input capacitance
Comparator

- Clock rate $f_s$
- Resolution
- Overload Recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- ...

CMOS Comparator Example

Comparator with Auto-Zero


Auto-Zero Implementation

Flash Converter Errors

- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time

- Comparator output:
  - Sparkle codes (... 11101000 ...)
  - Metastability

Sparkle Codes

Correct Output:
0110 ... 1000

Actual Output:
1110
Sparkle Tolerant Encoder

Protects against a single sparkle.


Meta Stability

Different gates interpret metastable output X differently

Correct Output: 0111 or 1000
Actual Output: 1111

Solutions:
- Latches (high power)
- Gray encoding

Gray Encoding

- Each $T_i$ affects only one $G_i$
  - Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

<table>
<thead>
<tr>
<th>Thermometer Code</th>
<th>Gray</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_1$ $T_2$ $T_3$ $T_4$ $T_5$ $T_6$ $T_7$</td>
<td>$G_3$ $G_2$ $G_1$</td>
<td>$B_3$ $B_2$ $B_1$</td>
</tr>
<tr>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>1 0 0 0 0 0 0</td>
<td>0 0 1 0 0 1</td>
<td></td>
</tr>
<tr>
<td>1 1 0 0 0 0 0</td>
<td>0 1 1 0 1 0</td>
<td></td>
</tr>
<tr>
<td>1 1 1 0 0 0 0</td>
<td>0 1 0 0 1 1</td>
<td></td>
</tr>
<tr>
<td>1 1 1 1 0 0 0</td>
<td>1 1 0 1 0 0</td>
<td></td>
</tr>
<tr>
<td>1 1 1 1 1 0 0</td>
<td>1 1 1 1 0 1</td>
<td></td>
</tr>
<tr>
<td>1 1 1 1 1 1 0</td>
<td>1 0 1 1 0 0</td>
<td></td>
</tr>
<tr>
<td>1 1 1 1 1 1 1</td>
<td>1 0 0 1 1 1</td>
<td></td>
</tr>
</tbody>
</table>

$G_1 = T_1 \overline{T_3} + T_5 \overline{T_7}$

$G_2 = T_2 \overline{T_6}$

$G_3 = T_4$

Reducing Complexity

E.g. 10-bit “straight” flash
- Input range: 0 ... 1V
- LSB = $\Delta$: ~ 1mV
- Comparators: 1023 with offset << LSB
- Input capacitance: 1023 * 100fF = 102pF
- Power: 1023 * 3mW = 3W

Techniques:
- Interpolation
- Folding
- Folding & Interpolation
- Two-step, pipelining
Interpolation

• Idea
  – Interpolation between preamp outputs
• Reduces number of preamps
  – Reduced input capacitance
  – Reduced area, power dissipation
• Same number of latches
• Important “side-benefit”
  – Decreased sensitivity to preamp offset
  – \( \rightarrow \) improved DNL

Simulink Model
Preamp Output

Zero crossings (to be detected by latches) at $V_{in} =$

\[ V_{ref1} = 1 \Delta \]
\[ V_{ref2} = 2 \Delta \]

Differential Preamp Output

Zero crossings at $V_{in} =$

\[ V_{ref1} = 1 \Delta \]
\[ V_{ref2} = 0.5 \times (1+2) \Delta \]
\[ V_{ref2} = 2 \Delta \]
Interpolation in Flash ADC

Half as many reference voltages and preamps

Resistive Interpolation

- Resistors produce additional levels
- With 4 resistors, the “interpolation factor” $M=8$ (ratio of latches/preamps)

### DNL Improvement

- Preamp offset distributed over $M$ resistively interpolated voltages:
  - Impact on DNL divided by $M$

- Latch offset divided by gain of preamp
  - Use "large" preamp gain ...

### Preamp Input Range

- Linear preamp input ranges must overlap
  - i.e. range $> \Delta$

- Sets upper bound on gain
  - $< < V_{DD} / \Delta$
### Measured Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10 b</td>
</tr>
<tr>
<td>Maximum conversion freq</td>
<td>300 MHz</td>
</tr>
<tr>
<td>Integral non-linearity</td>
<td>±1.0 LSB</td>
</tr>
<tr>
<td>Differential non-linearity</td>
<td>±0.4 LSB</td>
</tr>
<tr>
<td>SNR/THD</td>
<td>10MHz input: 56.5-59 dB</td>
</tr>
<tr>
<td></td>
<td>50MHz input: 48-47 dB</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>8 pF</td>
</tr>
<tr>
<td>Input range</td>
<td>2 V</td>
</tr>
<tr>
<td>Power supply</td>
<td>-5.2V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>4.0W</td>
</tr>
<tr>
<td>Chip size</td>
<td>9.0 x 4.2 mm²</td>
</tr>
<tr>
<td>Element count</td>
<td>36,000</td>
</tr>
<tr>
<td>Technology</td>
<td>1.0 µm bipolar: ft=25GHz</td>
</tr>
</tbody>
</table>


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### Folding Converter

- Significantly fewer comparators than flash \(\sim 2^{B/2+1}\)
- Fast
- Nonidealities in folder limit resolution to \(~10\) bits

![Folding Circuit Diagram](#)
Folding

- Folder maps input to smaller range
- MSB ADC determines which fold input is in
- LSB ADC determines position within fold
- Logic circuit combines LSB and MSB results

Generating Folds
Folding Circuit

CMOS Folder Output

Accurate only at zero-crossings

Lowdown →
Most folding ADCs do not actually use the folds, but only the zero-crossings!
Parallel Folders

Folder 4
\[ V_{in} = \frac{3}{4} \Delta \]
Fine Flash ADC 4

Folder 3
\[ V_{in} = \frac{2}{4} \Delta \]
Fine Flash ADC 3

Folder 2
\[ V_{in} = \frac{1}{4} \Delta \]
Fine Flash ADC 2

Folder 1
\[ V_{in} = 0 \Delta \]
Fine Flash ADC 1

Logic

Parallel Folder Outputs

- 4 Folders
- 8 Zero crossings
- \( \rightarrow \) only 3 LSB bits
- Better resolution
  - More folders
    - \( \rightarrow \) huge complexity
  - Interpolation
Folding & Interpolation

Folder 4
$V_{ref} + 3/4 \Delta$

Folder 3
$V_{ref} + 2/4 \Delta$

Folder 2
$V_{ref} + 1/4 \Delta$

Folder 1
$V_{ref} + 0/4 \Delta$

Encoder

Folder / Interpolator Output
Folder / Interpolator Output

Interpolate only between closely spaced folds to avoid nonlinear distortion.

A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter
B. Nauta and G. Venes, JSSC Dec 1985, pp. 1302-8
A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter

![Diagram of the converter](image)

### Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{DD}=5V$ $V_{ref}=3.3V$</td>
</tr>
<tr>
<td>Analog input</td>
<td>2Vpp, 1.4Vpp</td>
</tr>
<tr>
<td>Integral nonlinearity</td>
<td>±0.04LSB, ±0.02LSB</td>
</tr>
<tr>
<td>Differential nonlinearity</td>
<td>±0.02LSB, ±0.01LSB</td>
</tr>
<tr>
<td>Max. clock frequency</td>
<td>70MHz, 40MHz</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>119mW, 45mW</td>
</tr>
</tbody>
</table>