UNIVERSITY OF CALIFORNIA
College of Engineering
NTU 776CA (EECS 247)

Final (180 minutes)
December 10-14, 2001

Exam is open-book, open-notes. Clearly mark results with box around. No credit for ambiguous solutions. Show derivations. Return this cover page. Good luck!

Name: ____________________

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1. [40] Derive the Z-domain voltage transfer function $H(z)$ of the following switched-capacitor filter for both phases $\phi_1$ and $\phi_2$. You may assume the op amp is ideal with infinite gain and bandwidth. $V_{in}$ updates in $\phi_2$ and holds in $\phi_1$. $V_{out}$ changes during both $\phi_1$ and $\phi_2$.

a) Derive $H_1(z) = V_{out}/V_{in}$ during phase $\phi_1$. [20]

b) Derive $H_2(z) = V_{out}/V_{in}$ during phase $\phi_2$. [20]
2. Transition from $\phi_2 \rightarrow \phi_1$.

Sum charges on $C_1$, $C_2$, $C_4$. Apply charge conservation.

\[ V_{O2}(n) \cdot C_4 = V_{i1}(n+1) \cdot (C_1 + C_2) + V_{O1}(n+1) \cdot C_4 \]

\[ \Rightarrow \quad V_{O2}(z) \cdot C_4 = Z \cdot V_{i1}(z) \cdot (C_1 + C_2) + Z \cdot V_{O1}(z) \cdot C_4 \quad (***) \]

Solve (*) and (***), together,

\[ H_1(z) = \frac{V_{O1}(z)}{V_{i1}(z)} = \frac{C_1 + C_2 - C_1 \cdot z^{-1}}{(C_3 + C_4) \cdot z^{-1} - C_4} \]

\[ H_2(z) = \frac{V_{O2}(z)}{V_{i1}(z)} = H_1(z) \left( 1 + \frac{C_3}{C_4} \right) + \frac{C_1}{C_4} \]

\[ = \frac{C_1 + C_2 - C_1 \cdot z^{-1}}{(C_3 + C_4) \cdot z^{-1} - C_4} \left( 1 + \frac{C_3}{C_4} \right) + \frac{C_1}{C_4} \]
2. [20] In flash A/D converters, multi-stage preamp topology is usually adopted to reduce the comparator offset. In the following diagram, a three-stage cascaded inverter chain is used as the preamp. Assume $A1 = A2 = A3 = -4$ and each inverter has an input referred offset voltage $V_{osi}$. The comparator (latch) has an offset of $V_{os4}$. The inverters are auto-zeroed (input and output shorted before comparison is performed) to reduce the offsets of themselves. You may assume all switches are ideal.

![Diagram of preamp and latch](image)

a) Explain the functionality of capacitors $C1$ through $C3$. [5]

b) Derive an expression for the total input-referred offset voltage due to all preamps and the latch. [10]

c) If all offset voltages are roughly the same, which stage, in your opinion, contributes the most of the overall input-referred offset? Could you suggest a simple auto-zeroing circuit that further reduces this dominant offset error? [5]

\[ V_i - V_X = V_{os2} \]
\[ V_i = V_0 = AV_X \]
\[ V_i = V_0 = \frac{A}{A-1} V_{os} = \frac{4}{5} V_{os} \]

So, $V_{os, in} = \frac{4}{5} V_{osi} + \frac{V_{os4}}{64}$

c) $V_{osi}$ is the dominant offset source.

Revised version of preamp:

![Revised preamp diagram](image)
3. [40] The following circuit diagram shows a fast residue amplifier designed for digitally corrected 1-b/stage pipelined A/D converters. A single transistor amplifier exhibits very high speed, but suffers from finite DC gain effect and nonlinearity. Assume capacitors are perfectly matched (C1 = C2 = C). Input voltage is sampled in phase φ1 (note that the sampling operation also performs auto-zeroing) and amplified in phase φ2. In φ2, C2 is connected to either 0 or Vref depends on the Vin value. If Vin is below Vref/2 (comparator decision D = 0), then C2 is connected to 0; if it is above Vref/2 (comparator decision D = 1), then Vref. Ignore all parasitics. Assuming the digital correction algorithm is not applied, answer the following questions:

![Circuit Diagram]

a) If the open-loop gain of the amplifier formed by M1 and R is -A, derive a closed-form expression for the output residue voltage Vout in terms of Vin, Vref, and comparator decision D (you may assume Vgs of M1 is 1V when φ1 is closed). [20]

Hint: Note the quiescent biasing point of the amplifier is that when φ1 is closed. The open-loop gain is defined in terms of the signal swing where quiescent biasing is removed.

b) Suppose we use this residue amplifier in the 1st stage of a 10-bit pipelined A/D converter. If A = 40 is constant, how many missing codes are there around Vref/2 (assuming the following 9-bit converter is ideal and is designed to resolve out of range signals)? [20]
#3.  

a) Circuit in $\phi_1$:

\[ Q(\phi_1) = (V_i - V_{gs}) (C_1 + C_2) \]

b) Circuit in $\phi_2$:

\[ Q(\phi_2) = (DV_{ref} - V_x) C_2 + (V_o - V_x) C_1 \]

Apply charge conservation law: \[ Q(\phi_1) = Q(\phi_2) \]

Also note that in $\phi_2$: \[ -A (V_x - V_{gs}) = V_o - V_{gs} \]

Solve 1 & 2 together,

\[ V_o = \frac{V_i (C_1 + C_2) - DV_{ref} C_2 + \frac{V_{gs} (C_1 + C_2)}{A}}{C_1 + \frac{C_1 + C_2}{A}} \]

\[ C_1 = C_2 = C = 2V_i - DV_{ref} + \frac{2V_{gs}}{A} \]

(\text{Note in case } A = \infty, V_o = 2V_i - DV_{ref}, \text{ the ideal residue TF.})

b) Measure jump at $V_{ref}/2$ of residue plot.

\[ \Delta = \frac{V_{ref} + \frac{2}{A}}{1 + \frac{2}{A}} - \frac{2}{1 + \frac{2}{A}} = \frac{V_{ref}}{1 + \frac{2}{A}} = \frac{V_{ref}}{1.05} \]

\Rightarrow \text{# of missing codes} = \left(1 - \frac{V_{ref}}{1.05} / V_{ref}\right) \cdot 2^{10} \approx 24