1. Consider a 6-bit flash ADC with an ideal reference resistor string and $V_{\text{ref}} = 1\text{V}$. Assume that the comparators have an offset voltage with standard deviation $\sigma_{\text{os}} = 3\text{mV}$. What are the standard deviations of the converter’s worst case DNL and INL?

2. A 16-bit pipeline ADC is implemented with 1-bit stages (just one comparator per stage). What is the maximum interstage gain for which a $\pm 0.1\text{V}_{\text{ref}}$ comparator offset can be tolerated? How many stages are required to get 16-bit resolution? (Converter voltage range $\pm V_{\text{ref}}$)

   Hint: To simplify things, design each stage to produce a residue that never leaves the box for up to $\pm 0.1\text{V}_{\text{ref}}$ comparator offset.

3. The figure below shows one stage of a pipelined ADC. (Converter voltage range $\pm V_{\text{ref}}$)
   a) Plot $V_r$ as a function of $V_{\text{in}} / V_{\text{ref}}$.
   b) What is the maximum comparator offset relative to $V_{\text{ref}}$ that can be accommodated with digital error correction? Assume everything else is ideal.

4. Shown below is the schematic of an NMOS sampler used in the front-end of a B-bit ADC. The RC time constant of this circuit was chosen such that it settles to within 1 LSB in one half-clock period. R is the equivalent resistance of the switch. Derive an expression for the input referred total thermal noise of the sampler in terms of R, B, $f_s$, the Boltzmann constant and temperature.