UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
NTU IC-776CA

	Homework For Fun	**EECS 247**
B. E. BOSER	***Solution will be posted before final exam***	**Spring 2004**

You are to design a 2nd order sigma-delta modulator. Use the structure shown below. The DAC output levels are at $\pm V_{ref}$.

a) Modeling the quantizer as an additive white noise source, derive an equation for the SQNR as a function of oversampling ratio M. What oversampling ratio is required for 100dB SQNR? Round to the next higher power of two. What would be the minimum sampling frequency f_s to achieve a 20kHz signal bandwidth (assume a brick-wall filter)?

b) Verify the dynamic range with simulation. Use a small (e.g. -40dB) sinusoidal input and extrapolate to 0dB (see slide 19 in Lecture 16). Scale the horizontal axis such that 0dB corresponds to the power of a sinusoid with peak-to-peak amplitude $\pm V_{ref}$.

c) Plot the root-locus of the modulator as a function of effective quantizer gain G_{eff}. For what range of G_{eff} is the modulator stable?

d) Plot G_{eff} as a function of input power, using the same scale as in (b). What is the maximum input level for which the modulator is stable?

e) Scale the modulator internal nodes such that the peak integrator outputs do not exceed the DAC output levels for inputs up to -2dB. Plot the peak integrator outputs as a function of input amplitude for the scaled modulator.