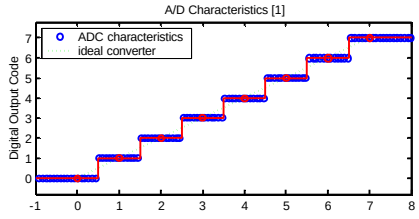
Amplitude Quantization

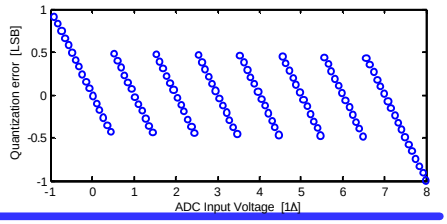
- Amplitude quantization
- Quantization “noise”
- Static ADC performance measures
  - Offset
  - Gain
  - INL
  - DNL
- ADC Testing
  - Code boundary servo
  - Histogram testing

Ideal Quantizer

- Quantization step Δ (= 1 LSB)
- N = 3 Bits
- Full-scale input range:
  $-0.5\Delta \ldots (2^N-0.5)\Delta$

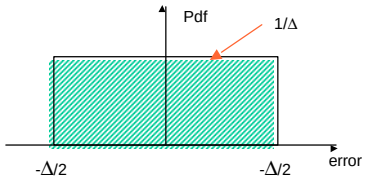


- Quantization error:
  bounded by $-\Delta/2 \ldots +\Delta/2$
  for inputs within full-scale range



Quantization Error PDF

- Uniformly distributed from $-\Delta/2 \ldots +\Delta/2$ provided that
  - Busy input
  - Amplitude is many LSBs
  - No overload
- Not Gaussian!



- Zero mean
- Variance

$$\overline{e^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12}$$

- Spectral density white if the joint pdf of the input at different sample times is smooth

Ref: W. R. Bennett, "Spectra of quantized signals," Bell Syst. Tech. J., vol. 27, pp. 446-72, July 1988.

B. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," IRE Trans. Circuit Theory, vol. CT-3, pp. 266-76, 1956.

Signal-to-Quantization Noise Ratio

- Since if some conditions are met (!) the quantization error is random, it is often referred to as "noise"
- In this case, we can define a peak "signal-to-quantization noise ratio", SQNR, for sinusoidal inputs:

$$SQNR = \frac{\frac{1}{2}\left(\frac{2^N \Delta}{2}\right)^2}{\frac{\Delta^2}{12}} = 1.5 \times 2^{2N}$$

$$= 6.02N + 1.76 \text{ dB}$$

e.g.	N	SQNR
	8	50 dB
	12	74 dB
	16	98 dB
	20	122 dB

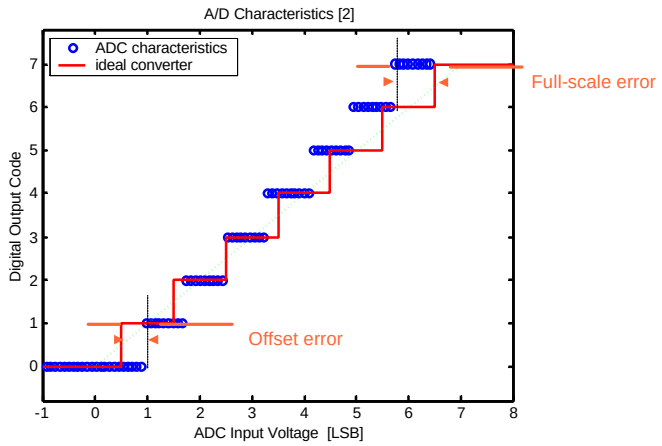
- Actual converters do not quite achieve this performance due to other errors, including
  - Electronic noise
  - Deviations from the ideal quantization levels

Static ADC Errors

Deviations of characteristic from ideal staircase

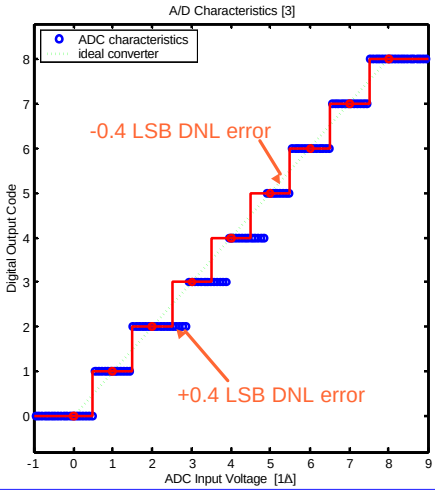
- Offset
- Gain error
- Differential Nonlinearity, DNL
- Integral Nonlinearity, INL

Offset and Gain Error

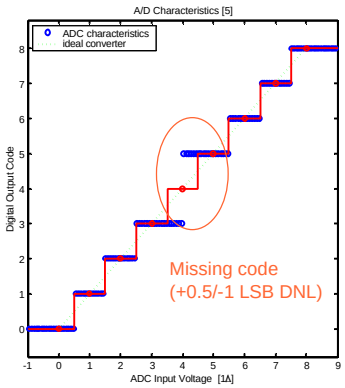


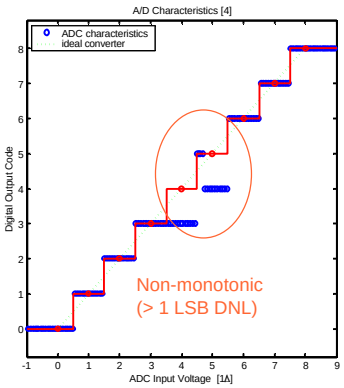
Differential Nonlinearity

DNL = deviation of bin width from Δ



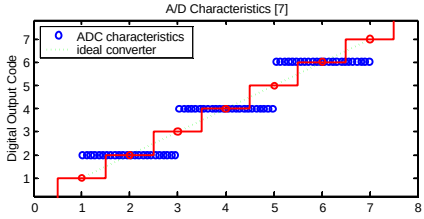
Differential Nonlinearity



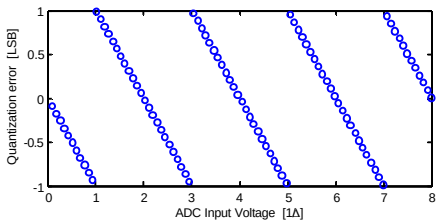


Large DNL Errors

A converter with DNL larger than 1LSB could be equivalent an ideal ADC with 1 bit less resolution

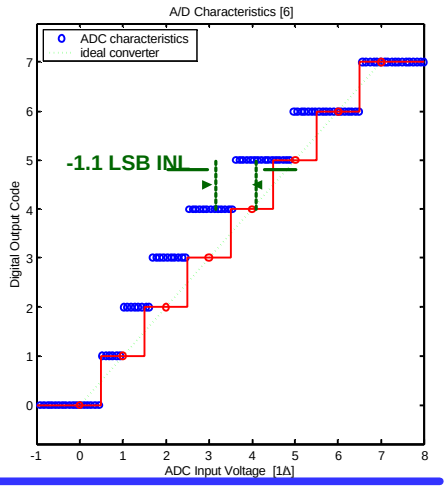


At right:
alternating DNL –1/+1 LSB



Integral Nonlinearity

- INL = deviation of actual center of bin from its ideal location
- A straight line through the endpoints is usually used as reference,
  i.e. offset and gain errors are ignored in INL calculation
- Note that INL errors can be much larger than DNL errors and vice-versa

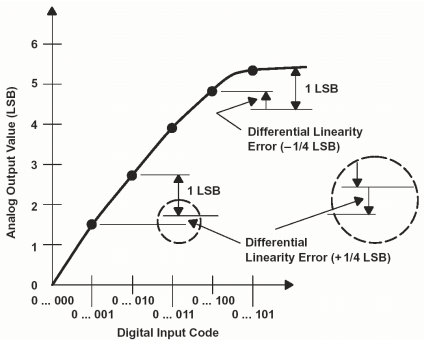


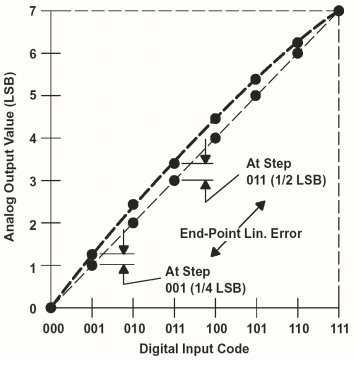
Monotonicity

- Monotonicity guaranteed if
  $$| INL | = 0.5 \text{ LSB}$$
  The best fit straight line is taken as the reference for determining the INL.
- This implies
  $$| DNL | = 1 \text{ LSB}$$
- Note: these conditions are sufficient but not necessary for monotonicity

- Ref: R. J. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic Publishers, 1994.

DAC DNL and INL



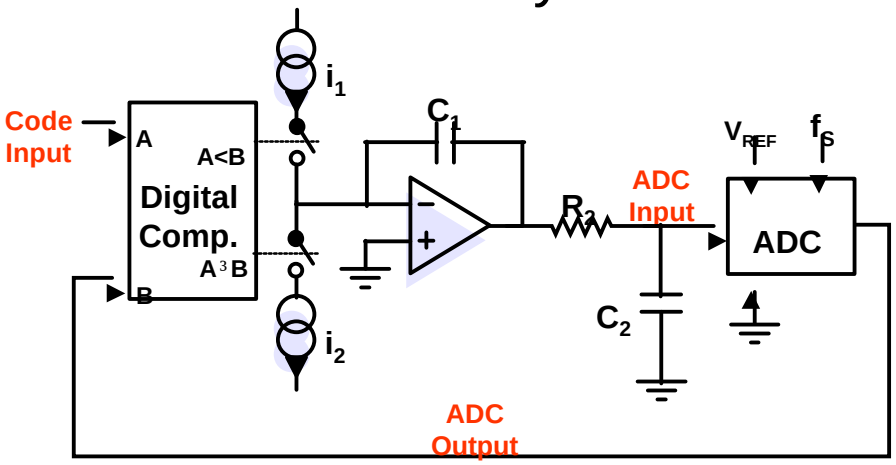


Ref: "Understanding Data Converters," Texas Instruments Application Report SLAA013, Mixed-Signal Products, 1995.

DNL and INL Testing

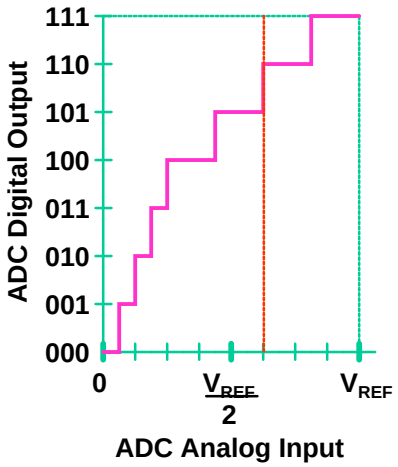
- Code boundary servo
- Code density (histogram) testing

Code Boundary Servo

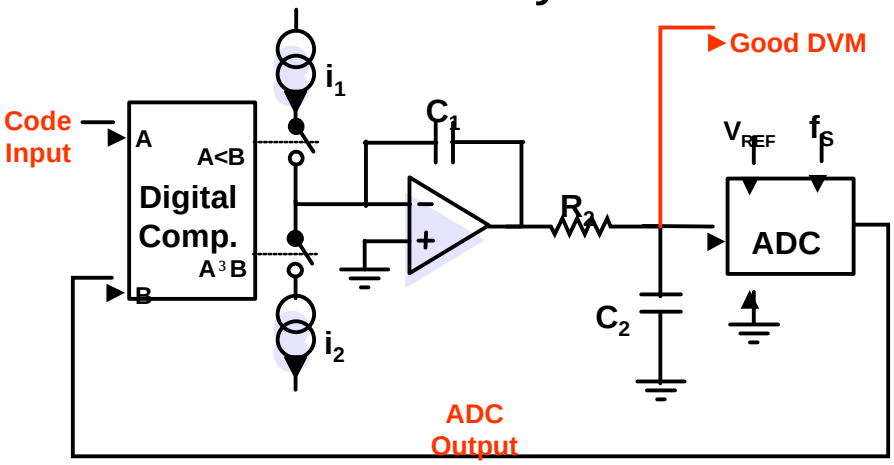


Code Boundary Servo

- i_1 and i_2 are small, and C_1 is large, so the ADC analog input moves a small fraction of an LSB each sampling period
- For a code input of 101, the ADC analog input settles to the code boundary shown



Code Boundary Servo



Code Boundary Servo

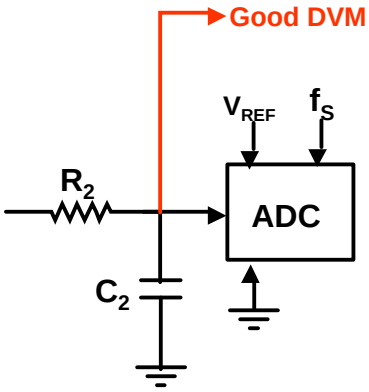
- A very good digital voltmeter (DVM) measures the analog input voltage corresponding to the desired code boundary
- DVMs have some interesting properties
  - They can have very high resolutions (8½ decimal digit meters are inexpensive)
  - To achieve stable readings, DVMs average voltage measurements over multiple 60Hz ac line cycles to filter out pickup in the measurement loop
  - 60Hz pickup in typical measurement loops is ~10mV

Code Boundary Servo

- A high-accuracy (as opposed to high-resolution) DVM is unnecessary
  - The same meter can measure the ADC's voltage reference
- A high-accuracy ADC reference voltage is likewise unnecessary
  - V_{REF} must be stable to within a fraction of an LSB for the duration of the INL test

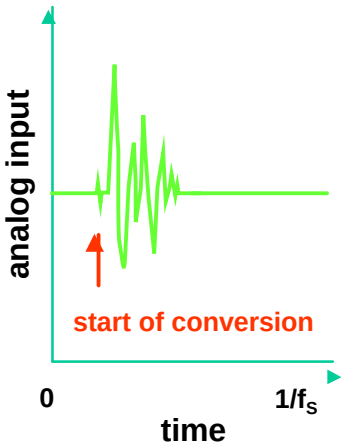
Code Boundary Servo

- ADCs of all kinds are notorious for kicking back high-frequency, signal-dependent glitches to their analog inputs
- A magnified view of an analog input glitch follows …



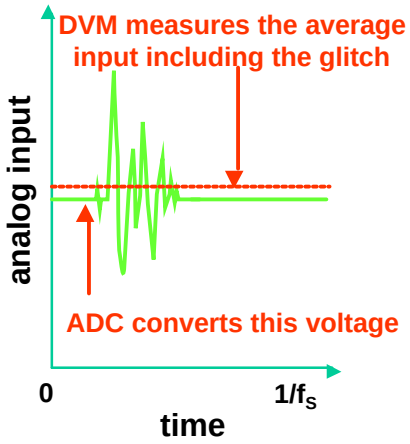
Code Boundary Servo

- Just before the input is sampled and conversion starts, the analog input is pretty quiet
- As the converter begins to quantize the signal, it kicks back charge



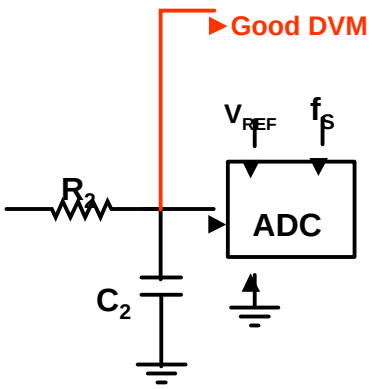
Code Boundary Servo

- The difference between what the ADC measures and what the DVM measures is not ADC INL, it's error in the INL measurement
- How do we control this error?



Code Boundary Servo

- A large C_2 fixes this
- At the expense of longer measurement time (the DVM is slow anyway)

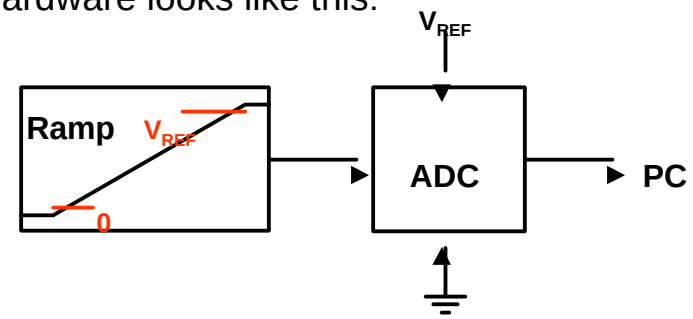


Histogram Testing

- Code boundary measurements are slow
  - Long testing time
  - May miss dynamic errors
- Histogram testing
  - Quantize input with known pdf (e.g. ramp or sinusoid)
  - Derive INL and DNL from deviation of measured pdf from expected result

Histogram Test Setup

- DNL is usually measured via a code frequency of occurrence histogram
- Hardware looks like this:



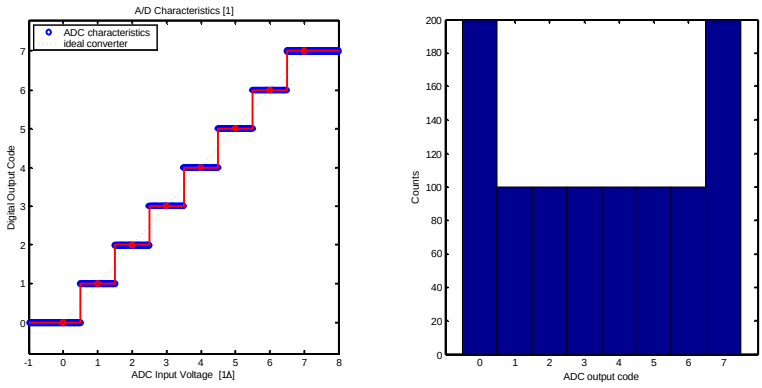
Measuring DNL Error

- Ramp speed is adjusted to provide an average of 100 outputs of each ADC code
  (for 1/100 LSB resolution)

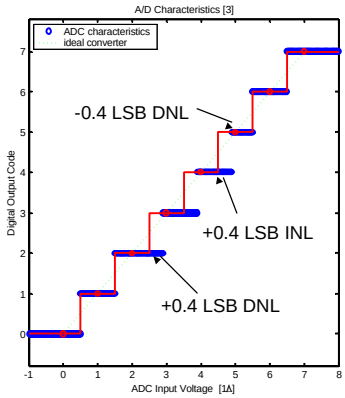
- Ramps can be quite slow for high resolution ADCs:

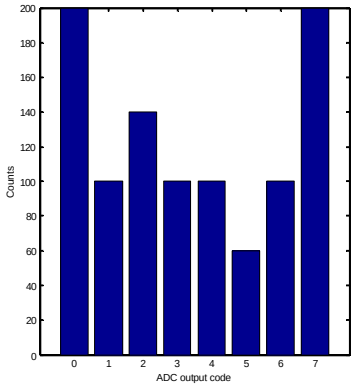
$$\frac{\textbf{(65536 codes)(100 conversions/code)}}{\textbf{100000 conversions/sec}} = \textbf{65.6 sec}$$

Histogram of Ideal 3 Bit ADC



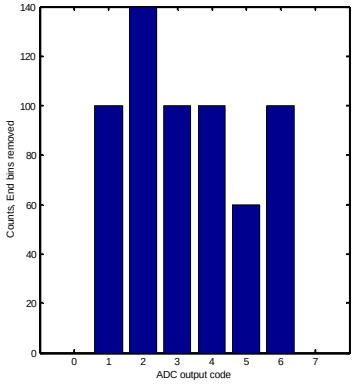
Histogram of Sample 3 Bit ADC





DNL from Histogram

Remove “over-range bins” (0 and 7)

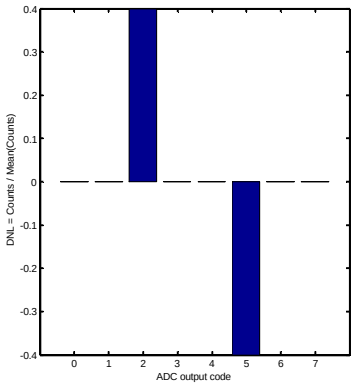


DNL from Histogram

Scale:

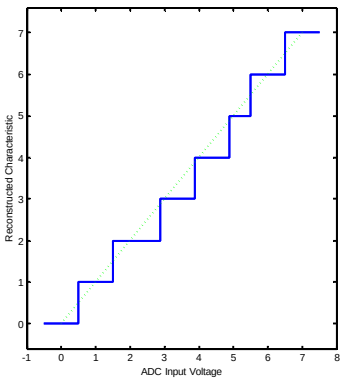
1. divide by average count
2. subtract 1
   (ideal bins have exactly the average count, which, after normalization, is 1)

Result is DNL

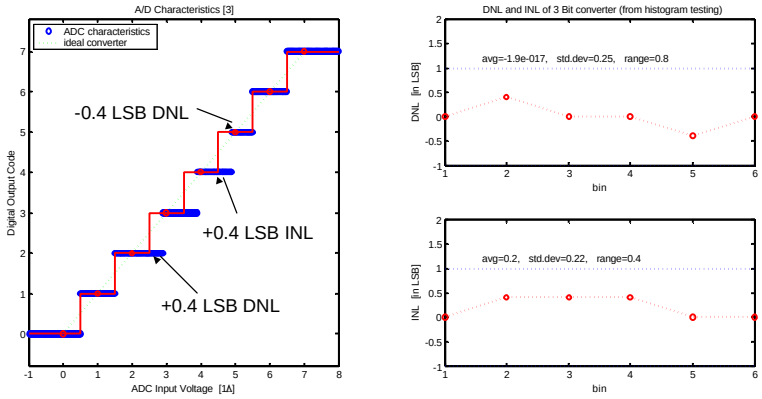


INL from Histogram

- The DNL tells us width of all bins (DNL + 1)
- We can use it to reconstruct the exact converter characteristic (having measured only the histogram) by simply adding up all bin-width'
- The INL is the deviation from a straight line through the end points

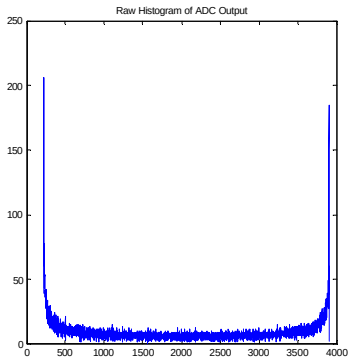


DNL and INL of Sample ADC



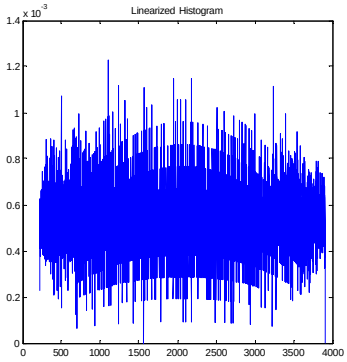
Sinusoidal Inputs

- Ramps are limited to slow inputs and may miss dynamic effects
- Solution: use sinusoidal test signal
- Problem: ideal histogram is not flat but has “bath-tub shape”

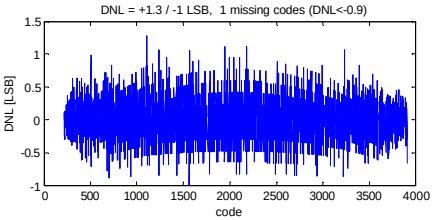


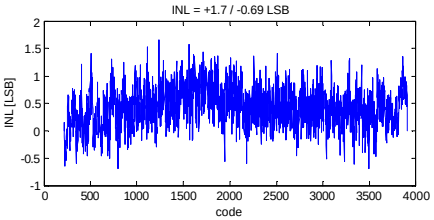
Sinusoidal Inputs

- After correction for "sinusoidal pdf"



DNL and INL





Ref: [1] M. V. Bossche, J. Schoukens, and J. Renneboog, "Dynamic Testing and Diagnostics of A/D Converters," IEEE Transactions on Circuits and Systems, vol. CAS-33, no. 8, Aug. 1986.

[2] IEEE Standard 1057

DNL/INL Code

```
function [dnl,inl] = dnl_inl_sin(y);
%DNL_INL_SIN
% dnl and inl ADC output
% input y contains the ADC output
% vector obtained from quantizing a
% sinusoid

% Boris Murmann, Aug 2002
% Bernhard Boser, Sept 2002

% histogram boundaries
minbin=min(y);
maxbin=max(y);

% histogram
h = hist(y, minbin:maxbin);

% cumulative histogram
ch = cumsum(h);

% transition levels
T = -cos(pi*ch/sum(h));

% linearized histogram
hlin = T(2:end) - T(1:end-1);

% truncate at least first and last
% bin, more if input did not clip ADC
trunc=2;
hlin_trunc = hlin(1+trunc:end-trunc);

% calculate lsb size and dnl
lsb= sum(hlin_trunc) / (length(hlin_trunc));
dnl= [0 hlin_trunc/lsb-1];
misscodes = length(find(dnl<-0.9));

% calculate inl
inl= cumsum(dnl);
```


DNL/INL Code Test

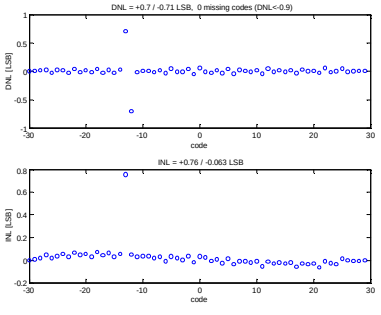
```
% converter model
B = 6;               % bits
range = 2^(B-1) - 1;
% thresholds (ideal converter)
th = -range:range;   % ideal thresholds
th(20) = th(20)+0.7; % error

fs = 1e6;
fx = 494e3 + pi;     % try fs/10!
C  = round(100 * 2^B / (fs / fx));

t = 0:1/fs:C/fx;
x = (range+1) * sin(2*pi*fx.*t);
y = adc(x, th) - 2^(B-1);

hist(y, min(y):max(y));

dnl_inl_sin(y);
```



Limitations of Histogram Testing

- The histogram (as any ADC test, of course) characterizes one particular converter. Test many devices to get valid statistics.
- Histogram testing assumes monotonicity.
  E.g. “code flips” will not be detected.
- Dynamic sparkle codes produce only minor DNL/INL errors.
  E.g. 123, 123, …, 123, 0, 124, 124, … → look at ADC output to detect.
- Noise not detected or improves DNL.
  E.g. 9, 9, 9, 10, 9, 9, 9, 10, 9, 10, 10, 10, …

Ref: B. Ginetti and P. Jespers, “Reliability of Code Density Test for High Resolution ADCs,” Electron. Lett., vol. 27, pp. 2231-3, Nov. 1991.