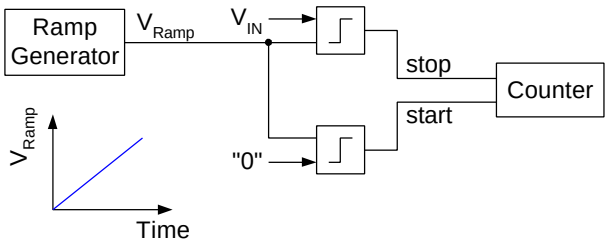
ADC Architectures

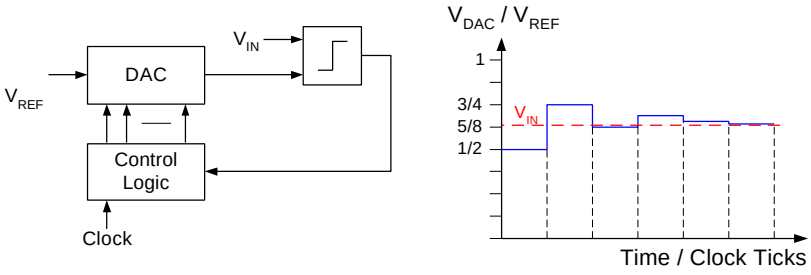
- Serial ADC
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - …
- Oversampled ADCs

Serial ADC



- Low complexity
- Very high accuracy achievable (digital volt-meter)
- Slow: conversion time proportional 2^B

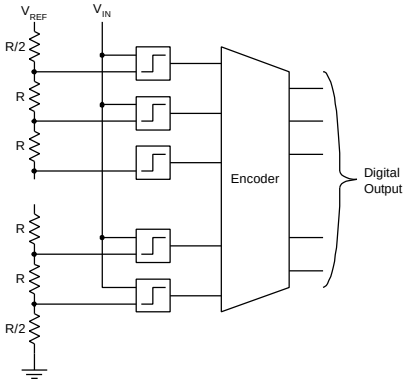
Successive Approximation



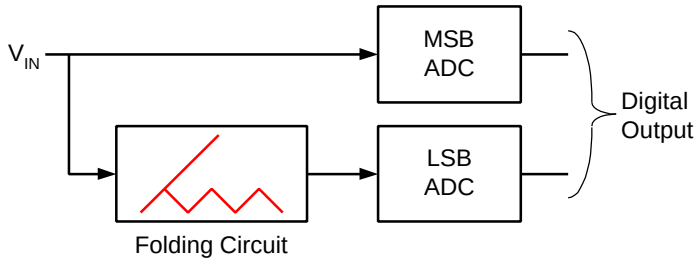
- Binary search over DAC output
- High accuracy achievable (16+ Bits)
- Moderate speed proportional to B (1+ MHz)

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance

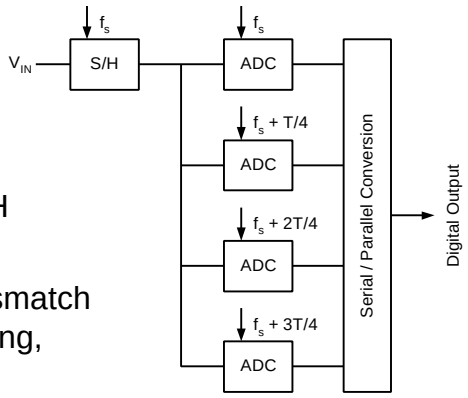


Folding Converter



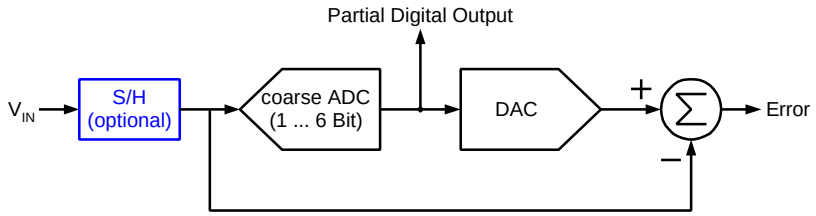
- Significantly fewer comparators than flash ~$2^{B/2+1}$
- Fast
- Nonidealities in folder limit resolution to ~10Bits

Time Interleaved Converter



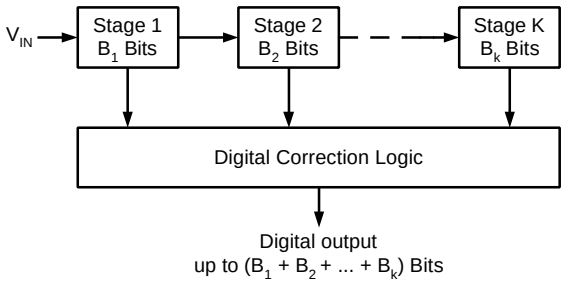
- Extremely fast:
  Limited by speed of S/H
- Accuracy limited by mismatch in individual ADCs (timing, offset, gain, …)

Residue Type ADC



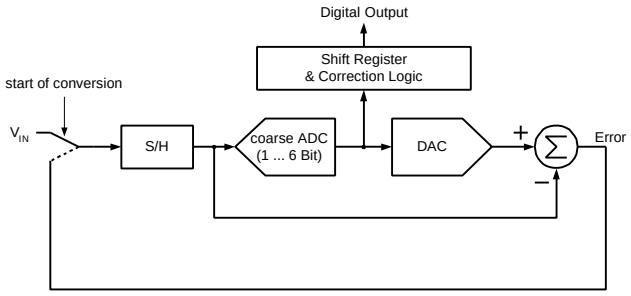
- Quantization error output (“residuum”) enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, …
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency

Pipelined ADC



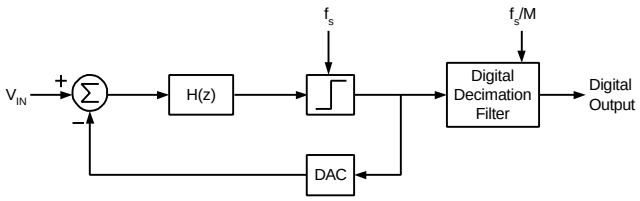
- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits / 1MS/s to 14Bits / 100MS/s

Algorithmic ADC



- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion

Oversampled ADC



- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

Speed Comparison