N247 HW4

S.Gambini

Shown in figure 1 below is the normalize prototype for a fourth order butterworth ladder filter.

- Denormalize the component values so as to obtain a bandwidth of 20MHz for $R_s = R_t = 1\Omega$. Subsequently, rescale all the component values to get a total integrated output noise of 1 mV rms
- Using the state-space signal flow graph approach described in lecture 6, obtain a leapfrog implementation of this filter using active-RC techniques
- Simulate your filter in cadence using an appropriate model for the opamp(See 2). Reduce the opamp gain-bandwidth product until you see 1dB passband gain error. What is the resulting GBW ?
- Tranform the filter into the switched-capacitor counterpart using LDI integrators.For the switched capacitor circuit, choose $F_s = 160MHz$. Compare your design to PSS+PAC analysis from SPECTRE (Use the switches analogLib sw in Cadence and set R_on and R_{off} to convenient values)
- After developing an appropriate model for the Gm cells, reduce the G_m of your transconductors, until when your simulations show a 1dB passband error compared to the simulaions of the discrete-time prototype, with all the transconductors having $G_m = 100mS$.

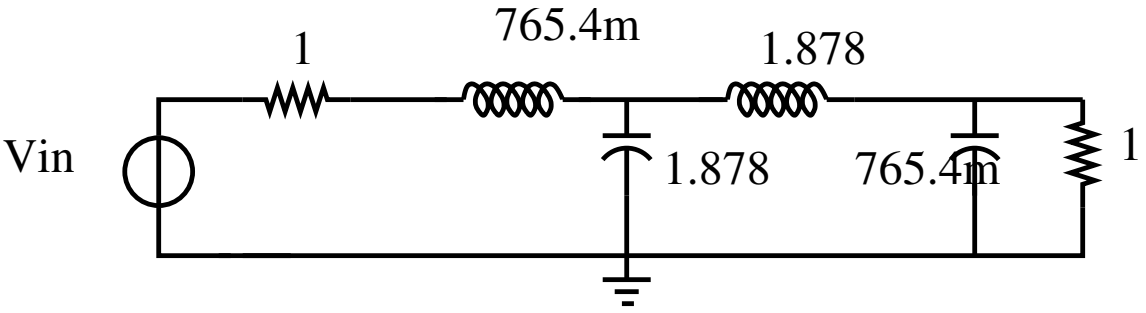

Fig. 1: Butterworth filter prototype

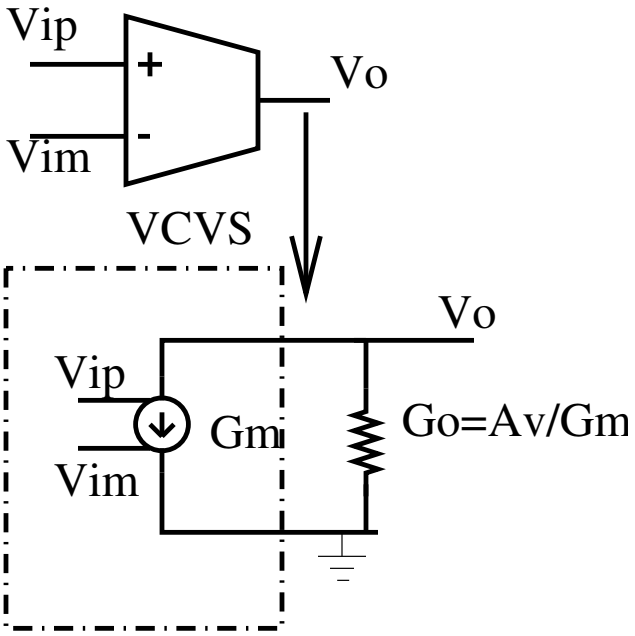

Fig. 2: Suggested OTA model

References

[1] T.Choi,R.W. Brodersen *Considerations for high-frequncy CMOS ladder filter* IEEE Transactions on Circuits and Systems,1980