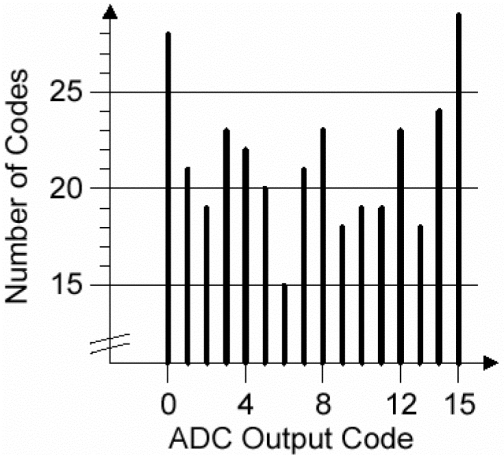
UNIVERITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
NTU 247

	Homework 4	**NTU 247**
B. E. Boser	**Due Monday, March 19, 2007**	**Spring 2007**

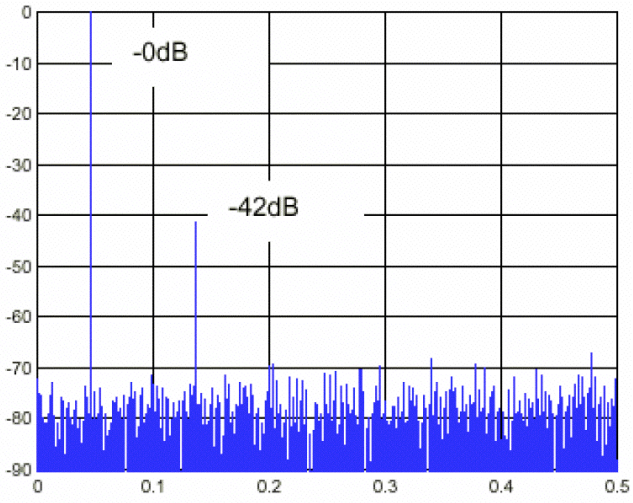
1. The graph below shows a histogram of the output codes obtained for a 4-bit ADC with a linear ramp input. Calculate the peak positive and negative DNL and INL in LSBs.



2. Shown below is a 4096-piont FFT of the output of an A/D converter for full-scale sinusoidal input. Estimate the INL of the converter in LSBs.

Note 1: *the definition of INL requires that the offset and gain of the ADC are adjusted for zero error at the end points (full scale);*

Note 2: $\sin^3\alpha = \frac{3}{4}\sin\alpha - \frac{1}{4}\sin 3\alpha$.



3. An R-string DAC is fabricated with resistors with $\sigma_{\Delta R/R} = 0.2\%$. For the INL and DNL to be better than 0.5LSB,

a) What is the expected yield of a 12-bit DAC?
b) What is the maximum achievable resolution (no trimming or calibration), if a yield of 99% good parts is desired?

4. Consider a 6-bit flash ADC with an ideal reference resistor string and $V_{ref} = 1V$. Assume that the comparators have an offset voltage with standard deviation $\sigma_{OS} = 3mV$. What are the standard deviations of the converter's worst case DNL and INL?

5. The figure below shows one stage of a pipelined ADC. (Converter voltage range: $\pm V_{ref}$.)

a) Plot V_r as a function of V_{in}/V_{ref};
b) What is the maximum comparator offset relative to V_{ref} that can be accommodated with digital error correction? Assume everything else is ideal.