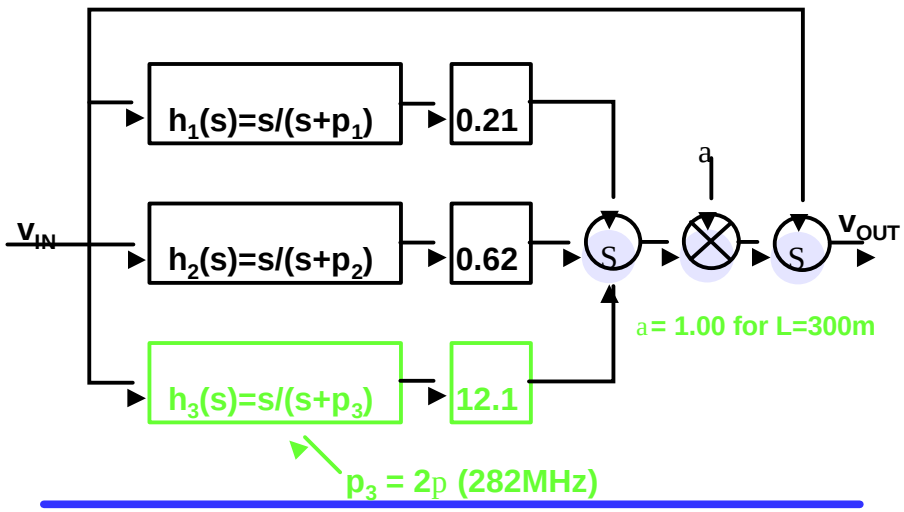
Offset Control

- Offset control in data receivers
  - dc offset
  - ac coupling
  - Baseline wander
  - Quantized feedback
- Decision circuits

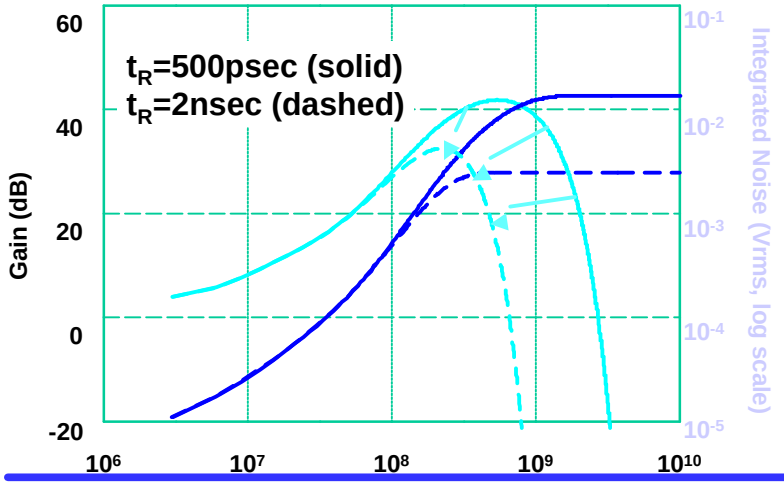
Equalizer Gain



Equalizer Gain

- Comlinear's cable equalizer uses 2 of the 3-pole sections in cascade
  - the highest value of equalizer gain appears to approach 12.1^2=43dB at high frequencies
- In practice, equalizer bandlimiting is required to limit noise and achieve acceptable bit error rates
  - maximum equalizer gain falls to about 32dB …

300m Equalizer Response



Equalizer Offsets

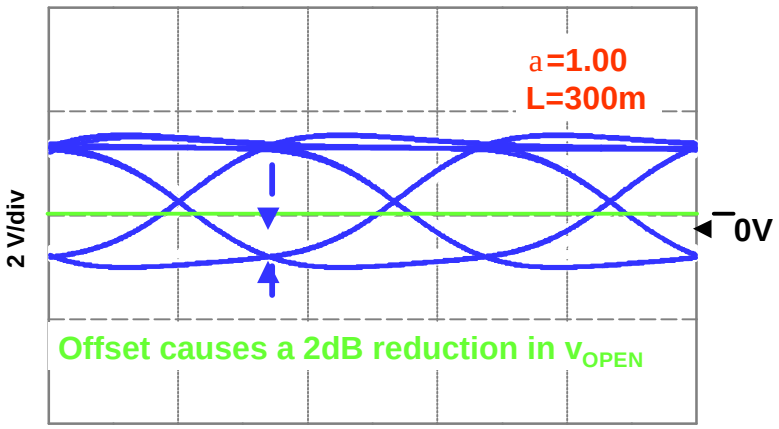
- Almost all data equalizers provide gain to compensate for channel losses
  - This gain also gains up offsets arising from device mismatches in amplifier stages
  - Typical high-speed amplifier stages have ~10mV input-referred offsets
- Most implementations of the Comlinear equalizer provide that gain (43dB) also to dc offsets
  - Left uncorrected, a 10mV input-referred offset becomes a 1.5V output offset …

Offset Eye Diagrams

Equalizer Offsets

- Even modest offsets can reduce the effective eye opening significantly
- The resulting effect on P_E can be severe
- The offset in the next slide results in a substantial bias in favor of -1→+1 errors …

Offset Eye Diagrams



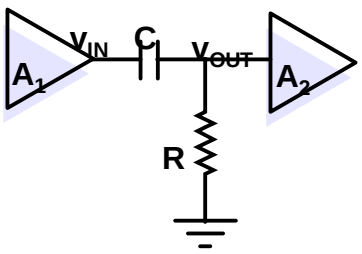
Equalizer Offsets

- Offset control is an important and under-appreciated component of data receiver architecture
  - The catch is that offsets must be controlled without slowing down the signal path
  - Offset control schemes often take as much design time as equalization itself
    - Initial design schedules typically underestimate this effort by wide margins

ac Coupling

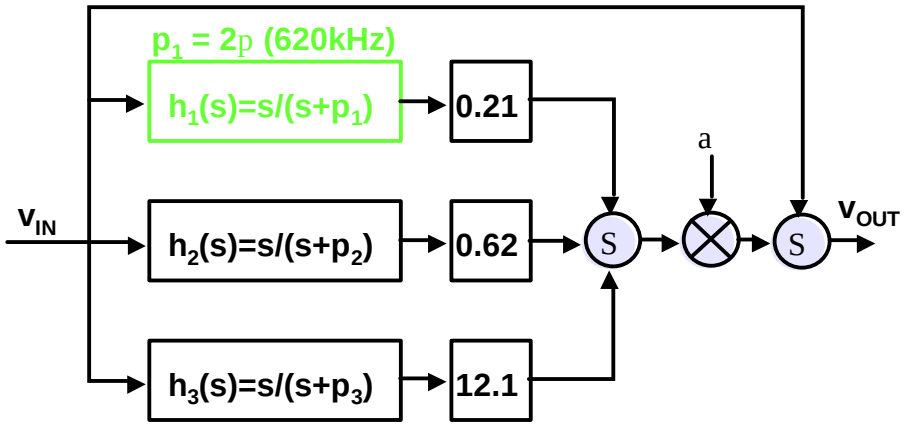
- ac coupling between amplifier stages is an obvious form of offset control:

$$H(s) = \frac{s}{s + \omega_P}$$



- Where should we set the HPF corner frequency?

Comlinear 3-Pole Section



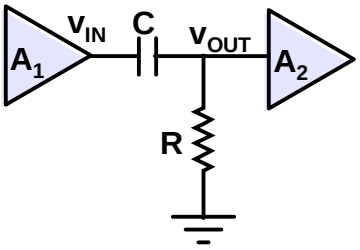
phase equalization provided by p_1 ends below 62kHz

ac Coupling

- A 10MΩ, 2.5pF ac coupling network (τ=RC=25μsec) can remove dc offsets from the Comlinear equalizer without much effect on its phase response above 62kHz
  - The large "resistor" can be realized with a long, narrow FET
- Does the high pass filter's own frequency response create any new problems in the NRZ data receiver?
  - The answer is "yes"
  - The problem is called "baseline wander"

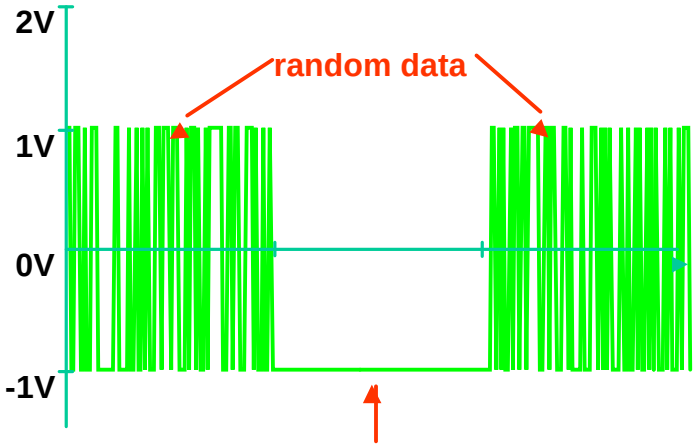
Baseline Wander

- Suppose our NRZ data stream comes from a sparsely populated binary file with lots of consecutive zeros in it
- We'll model the data stream as
  - 100µsec of random ±1V data at 300Mb/s
  - 100µsec of a fixed –1V level (models 30000 zeros in a row)

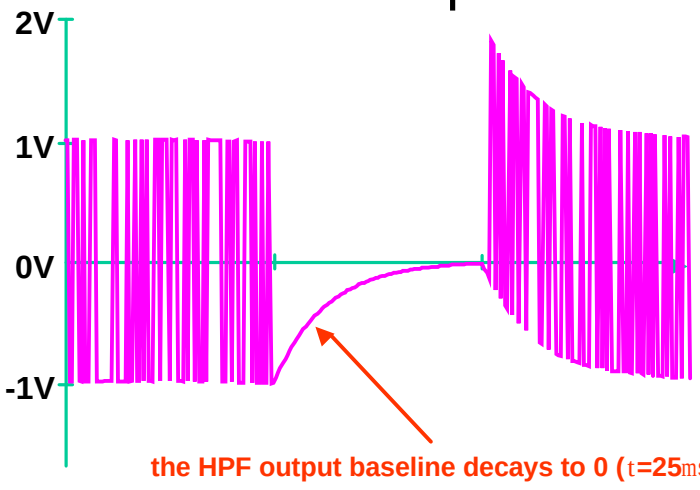


$$H(s) = \frac{s}{s + \omega_P}$$

Sparse HPF Input Data



HPF Output



Baseline Wander

- The high pass filter causes the middle of the data eye to wander with low frequency components in the NRZ data stream
  - Common data idling patterns move decision thresholds to the edges of the data eye
    - With disastrous consequences for bit error rates
  - Localized concentrations of –1's or +1's lasting on the order of 0.05τ reduce eye opening 0.5dB
    - Substantially increasing bit error rates
- What can we do about it?

Baseline Wander

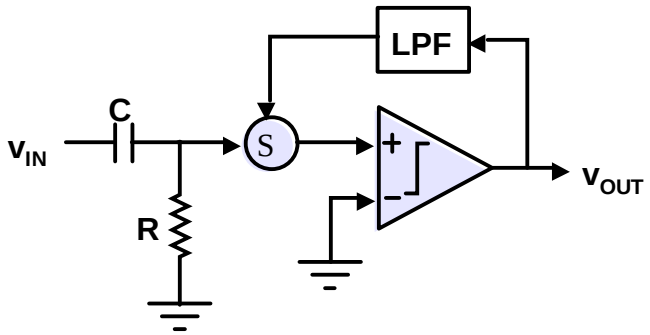
- Data scrambling can reduce the probability of perverse patterns
  - Common sparse sequences are mapped to transition-rich sequences
  - With 1:1 mapping, some irregular sequence will still map to a perverse baseline sequence, and the resulting baseline wander will cause errors
- Coding tricks can add extra bits to the data stream to ensure transition density
  - An 8b-9b code maps 8 data bits to 9 transmitted bits, with sparse patterns omitted from the 9b patterns
  - NRZ data throughput is reduced by the 8/9 factor

Quantized Feedback

- The problem is that the HPF assumes the data sequence has zero mean
- If we knew the data sequence, we could of course calculate this mean and add it to the HPF output
- Do we?
  - It appears at the output of the receiver …

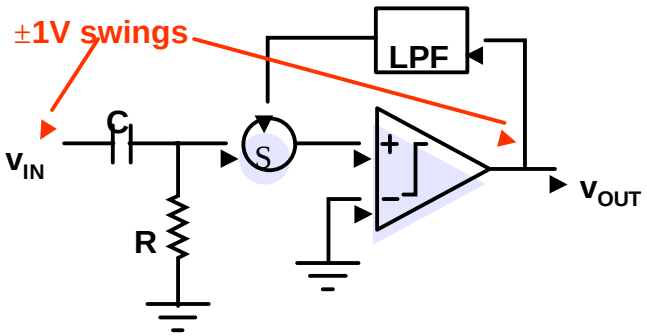
Quantized Feedback

- Quantized feedback combines a decision circuit (a comparator) and an ac coupling network in an ingenious way [2]:



Quantized Feedback

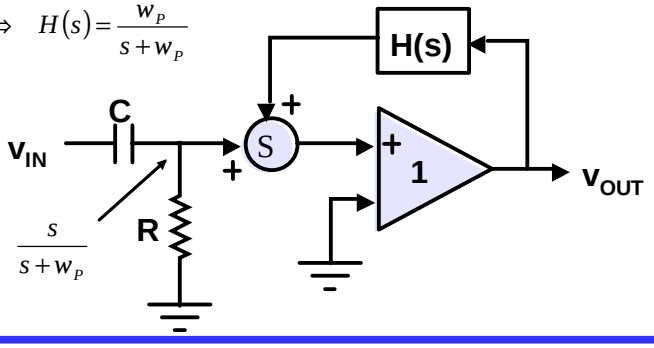
- The comparator is designed to produce the same p-p output swing as v_{IN}:



Quantized Feedback

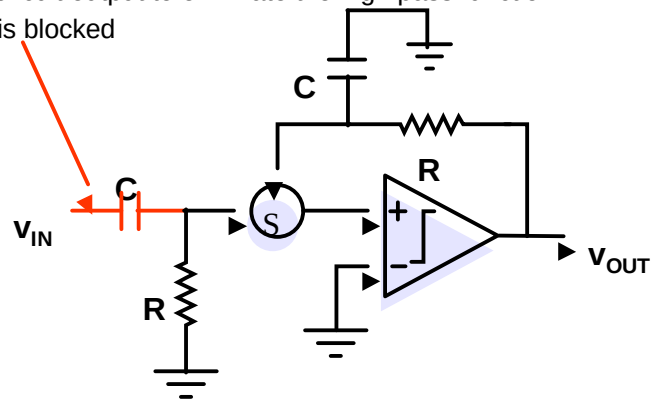
- How should we set the bandwidth of the LPF?
  - Model the quantizer as a gain (=1)
  - We want $V_{OUT} = V_{IN}$
  - Solve …

$$\Rightarrow \quad H(s) = \frac{w_P}{s + w_P}$$



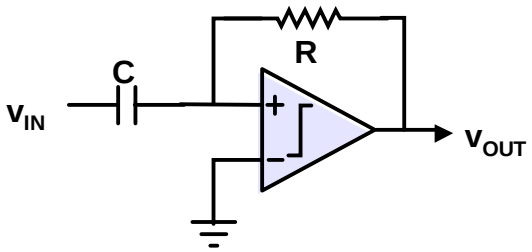
Quantized Feedback

- Quantized feedback uses a low pass filtered version of the decision circuit output to eliminate the high pass function
- dc offset is blocked

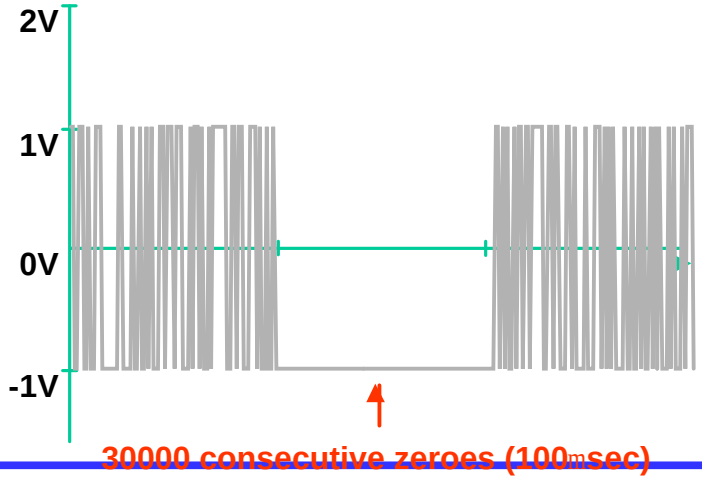


Quantized Feedback

- Though not as simple to visualize, the simplified circuit below does precisely the same thing

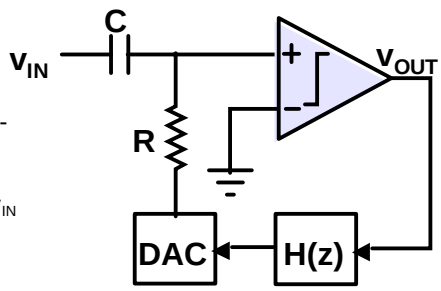


Quantized Feedback Output



Digital Quantized Feedback

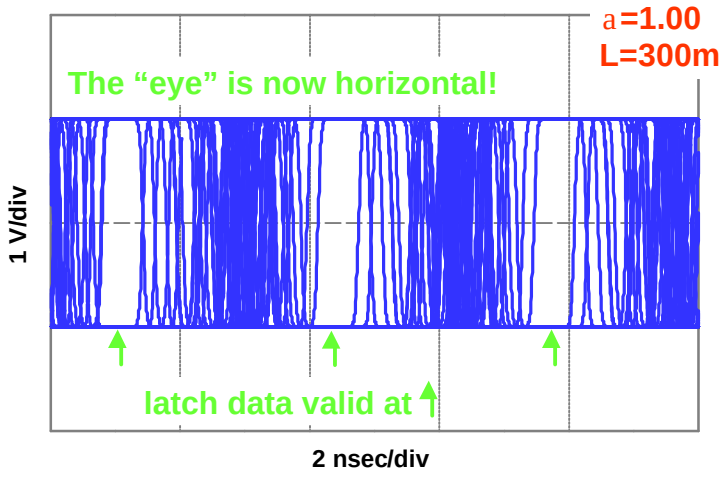
- Analog-digital hybrids can also provide baseline wander correction
- The H(z) block maps a logic-level v_{OUT} to channel signal levels
  - 6-7 DAC bits span the full v_{IN} range
- Startup and v_{IN}-v_{OUT} level mismatches must be carefully modeled



Decision Circuits

- Decision circuits generate square wave outputs at the output of the receiver
  - The square wave outputs typically drive a clocked, cross-coupled CMOS latch which produces full logic level swings [4]
- Decision circuits convert all sources of vertical eye degradation into horizontal eye degradation
  - A decision circuit's output transitions between two binary levels at a process-limited (NOT a data rate-limited) speed

Decision Circuit Eye Diagram



Decision Circuit Eye Diagram

- Obviously the bit error rate depends critically on the position of the green arrows
  - Those are generated by the clock recovery circuit
  - Typically those use an analog or digital PLL
  - We will leave that for 142!

The End

- We've looked at filters, converters, communication circuits …
- But especially we looked at how to model them
  - To come up with good architectures
  - To invent at the architecture level
  - To evaluate system performance at a high level where changes are manageable
- Good luck and good circuits, and thanks for taking my class!

References

1. Alan Baker, "An Adaptive Cable Equalizer for Serial Digital Video Rates to 400Mb/sec", ISSCC Dig. Tech. Papers, 39, 1996, pp. 174-175.
2. F. D. Waldhauer, "Quantized Feedback in an Experimental 280Mb/s Digital Repeater for Coaxial Transmission", IEEE Trans. on Communications, COM-22, January 1974, pp. 1-5.
3. Dave Pietruszynski, John Steininger, and E. J. Swanson, "A 50Mbit/sec CMOS Monolithic Optical Receiver", IEEE JSSC, SC-23, December 1988.
4. Akira Yukawa, "A CMOS 8-Bit, High-Speed A/D Converter IC", IEEE JSSC, SC-20, June 1985.