N247 Midterm Examination

S.Gambini

1. Shown below (1) is an active-RC integrator, where the operational amplifier is assumed to have a tranfer function of the form

$$A_v(s) = \frac{A_{v0}}{1 + s/s_p}$$

. A metric to evaluate how good the operational amplifier is is to define an integrator quality factor Q as $Q = \frac{\omega\tau}{q}$ where the integrator frequency response is $\frac{1}{j\omega\tau+q}$. Calculate the Q of this integrator separetely for the case in which $s_p = \infty$ and for the case in which $A_{v0} \to \infty, s_p \to 0, A_{v0} \cdot s_p \to \omega_u \leq \infty$. Suggest a circuit technique to improve the Q that does not require changing the opamp structure.

2. The circuit in figure 2 is used in integrated continuous-time filters to tune the center frequency of the filter to a specified value, made precise by the presence of the crystal oscillator OSC1. G_m1 and G_m2 are replicas of the filter transconductors, and are controlled by the same tuning voltage as the main transconductors. Explain qualitatively(alhtough in a NEAT way) the circuit operation and highlight the phase of the signals at nodes X and Y in the loop relative to the reference when the loop converged.

3. Your friend from Stanford says he can build a second order low-pass filter using 1 resistor R, 1 capacitor C and 1 operational amplifier. The opera-

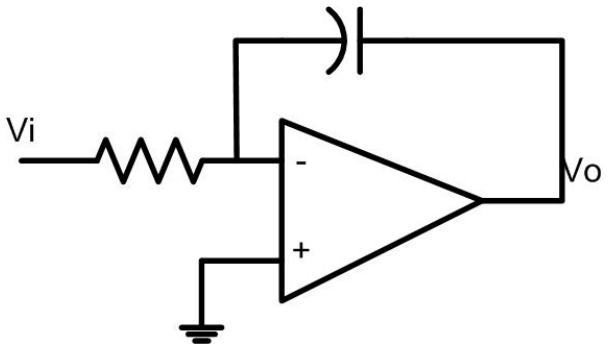

Fig. 1: Active-RC Integrator

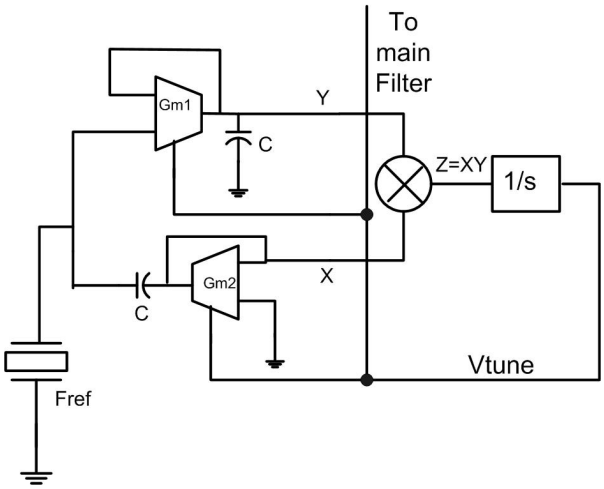

Fig. 2: Integrated Filter Tuning Circuit

tional amplifier will be generated as an IP block with transfer function

$$A_v(s) = \frac{A_{v0}}{1 + s/s_p}$$

, where A_{v0} and s_p can be chosen by you arbitrarily. Calculate explicitly the filter parameters obtainable as a function of R,C, A_{v0} and s_p. Are you really using only 1 capacitor? exaplain.

4. The circuit shown in figure 3 below must be used in the front end sample and hold for a 12 bit-75MS/s Nyquist rate A/D converter. The differential zero-peak swing at the input of the converter is 300mV, and the common mode input is 300mV. The switches are implemented as a single NMOS device and has an on resistance of the form $R(V_{in}) = \frac{R_0}{1-V_{in}}$. You are allowed to spend half of your 74dB the error budget on sampling noise, the other half being devoted to settling errrors; while the error due to sampling jitter should be at least at -80dB. Calculate the values of the sampling capacitor C, the resistance parameter R_0, and the maximum clock jitter variance that can be tolerated.

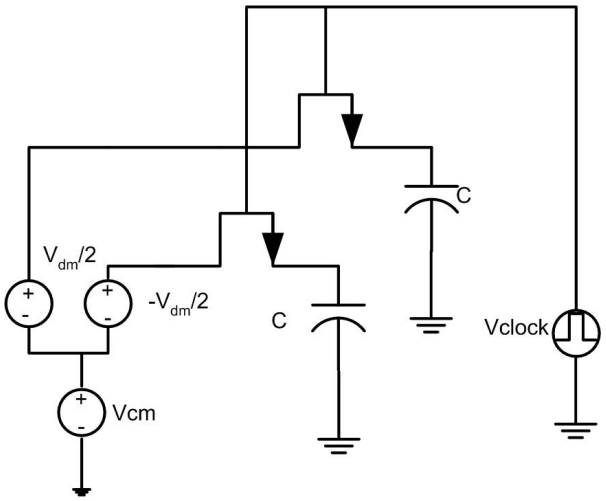

Fig. 3: Sampling Front End