N247 Midterm Examination Solution

S.Gambini

1. It can be shown that the general tranfer function of this block is

$$\frac{V_o}{V_i} = \frac{1}{RC_I s}(1 + (1 + \frac{1}{RC_I s})\frac{1}{A_v(s)})^{-1}$$

.For the case $Av(s) = A_{v0}$(finite gain flat gain) This simplifies to

$$\frac{V_o}{V_i} = \frac{1}{sRC_I(1 + \frac{1}{A_{v0}}) + \frac{1}{A_{v0}}}$$

and

$$Q = \omega RC_I(A_{v0} + 1)$$

.Therefore, the Q is proportional to frequency as should be expected(Losses are frequency independent, capacitive energy storage increses with frequency). For the case $A_v(s) = \frac{\omega_u}{s}$(Finite speed, infinite DC gain), this expression simplifies to(already in $j\omega$)

$$\frac{V_o}{V_i} = \frac{\omega_u}{j\omega(RC_I\omega_u + 1) - \omega^2 RC_I}$$

and

$$Q = \frac{-(RC_I\omega_u + 1)}{\omega RC_I}$$

. Notice that Q is here negative and decreasing with frequency (as opamp gain degrades with frequency in this case). To improve the Q, the nulling resistor technique should be used. Place a resistor in series with C_I such that $R_z C_I = \frac{1}{\omega_u}$.

2. To understand the behavior of the loop, two key observations must be done. The first one, is that Gm stage Gm_1 and capacitor C_1 for a low pass filter, while Gm_2 and C_2 a high pass filter. Assuming $Gm_1 = Gm_2 = Gm$, $C_1 = C_2 = C$, these two filters have transfer functions given by

$$\frac{V_{o1}}{V_{i1}} = \frac{1}{s/sp + 1} \tag{1}$$

$$\frac{V_{o1}}{V_{i1}} = \frac{s/s_z}{s/sp + 1} \tag{2}$$

Where $sp = \frac{Gm}{C}$. The second one is that the integrator(1/s block) in the loop enforces its input to have 0 mean. Since the input to the circuit is

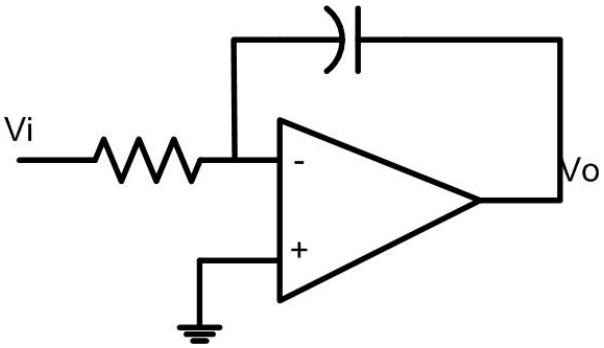

Fig. 1: Active-RC Integrator

sinusoidal(generated by the crystal), and the integrator is preceded by a multiplier, the multiplier inputs have to in quadrature for this to happen(in other words, they must have 90 degrees phase shift. In orger for this to happen, we must have $2\pi F_i = sp$. As in this condition, the output of the high pass filter leads its input by 45 degrees, while the output of the low pass filter lags its input by 45 degrees, resulting in the desired 90 degrees phase shift. Therefore, the integrator adjusts the value of the Gm until this condition is met.Notice the very important property of this scheme, which is shared by most of the tuning schemes for integrated analog filters: tuning is performed on Gm_1 and Gm_2 which ARE NOT EMPLOYED in the main filter, but are assumed to match closely the transconductors used in the main filter. Therefore, this tuning method has a finite accuracy, that limits the achievable Q with this strategy. Bonus question: would it make sense to apply this tuning strategy to a discrete filter?

3. The qualitative answer is that building such a second order filter is possible, even though we are not employing a single capacitor as physically we are using the internal capacitor of the opamp to set its pole. Filters realized this way are called Active-R and have been subject of research in 70s and also in the recent years (See paper by D'Amico in JSSC December 2006).Bonus question: Does this technique lend itself better to integrated or to discrete filters?. Using circuit topology and equations from Problem 1, it can be shown that the tranfer function is

$$H(s) = \frac{A_{v0}}{RC_I s^2 + s(RC_I(A_{v0}+1) + \frac{1}{sp}) + 1}$$

. Since a general second order low pass transfer function is characterized by three parameters (i.e., it can be written as $H(s) = \frac{G}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1}$, and we have 4 parameters available (R, C_I, A_{v0}, s_p), it is worth looking at what

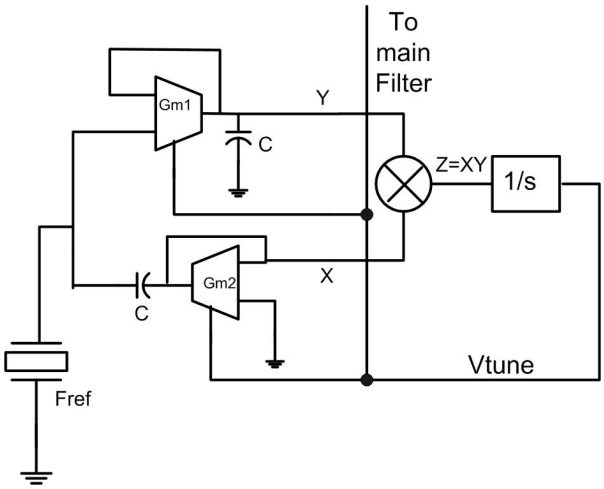

Fig. 2: Integrated Filter Tuning Circuit

kind filters can be built using this technique.We find

$$\omega_0 = (\frac{RC_I}{s_p})^{-1/2} \tag{3}$$

$$G = A_{v0} \tag{4}$$

$$Q = \frac{(s_p RC_I)^{1/2}}{(A_{v0}+1)RC_I s_p + 1} \tag{5}$$

4. Since the 74dB error budget is split equally between noise and settling error, each of them should be 3dB lower (-77dB). For noise, we have

$$\frac{2KT}{C} \leq \frac{V_{fs}^2}{2} 10^{-7.7} \rightarrow C \geq 8.9pF$$

(The factor of 2 stems from differential operation).For settling,we must have

$$V_{fs} e^{-\frac{T_s}{2\tau}} \leq V_{fs} 10^{-77/20} \rightarrow \tau \leq \frac{20 \cdot T_s}{2 \cdot 77 \cdot \ln(10)} = 750pS$$

. Since $\tau = RC$, we set $R \leq \frac{\tau}{C} = 85\Omega$ for all possible input values. For the given switch topology, the worst case is for $V_{in} = V_{cm} + V_{sw}/2 = 450mV$ and results in $R_0 = R(1-0.45) = 46\Omega$ For jitter, using the formula in the lecture, we have

$$-20\log_{10}(F_s \tau_J) - 5.172 \leq -80 \rightarrow \tau_J \leq \frac{1}{F_s} 10^{-74.82/20} = 2.6pS$$

NOTE: THIS IS A SPECIFICATION FOT THE ZERO-PEAK JITTER NOT FOR THE JITTER VARIANCE.

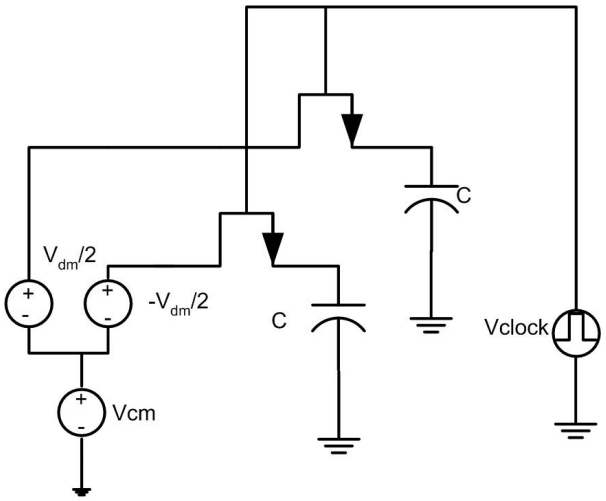

Fig. 3: Sampling Front End