10.1 MOS Physics
An NMOS device produces a current of 50 µA when operated at $V_{GS}=3V$ and $V_{DS}=3V$. The device has $W/L=2$, $V_T=1V$, and p-substrate doping $N_A=10^{16}$ cm$^{-3}$. The electric permittivity of Silicon dioxide is about $\varepsilon_{ox}=3.9*\varepsilon_0$, where $\varepsilon_0$ is the electric permittivity of free space.

a. Find the device parameters $\mu_n$, $C_{ox}$, and $t_{ox}$, assuming a pinch-off saturation behavior.

b. Find the device parameters $\mu_n$, $C_{ox}$, and $t_{ox}$, assuming a velocity saturation behavior with $V_{DSAT}=1.5V$.

c. Compare the current in the two devices from parts (a) and (b) when operated at $V_{GS}=1.5V$ and $V_{DS}=3V$. (Hint: Remember that MOSFET current saturates for $V_{DS} \geq \min(V_{GS}-V_T, V_{DSAT})$, where $V_{GS}-V_T$ is the condition for pinch-off and $V_{DSAT}$ is the condition for velocity saturation.)

10.2 NMOS Inverter
For the circuit shown in Figure 1, answer the following questions, using the NMOS_4XVS model given in Lecture 27.

a. Plot $I_O$ vs. $V_{OUT}$ for both the pull-up and pull-down devices for $V_{IN}=1V$, 2V, and 3V.

b. Plot the voltage transfer characteristic (VTC), $V_{OUT}$ vs. $V_{IN}$. What is the minimum $V_{OUT}$ for this inverter? How can you change $R_D$ to lower this value?

c. Find the power in the pull-up and pull-down devices when $V_{IN}=0V$ and $V_{IN}=3V$.

10.3 CMOS Inverter
For the circuit shown in Figure 2, answer the following questions, using the NMOS_4XVS model given in Lecture 27 and the PMOS_4XVS model given in Lecture 28.

a. Plot $I_O$ vs. $V_{OUT}$ for both the pull-up and pull-down devices for $V_{IN}=1V$, 1.25V, 1.5V, 1.75V, and 2V.

b. Plot the voltage transfer characteristic (VTC), $V_{OUT}$ vs. $V_{IN}$. What is output voltage range for this inverter?

c. Find the power in the pull-up and pull-down devices when $V_{IN}=0V$ and $V_{IN}=3V$. How does the power consumption of the CMOS inverter compare to the NMOS inverter?