Checkpoint 3 (1)
- You will get FULL MOTION video running on the board
  - 320x240 Black and White
  - 30 frames/30 fields per second
- This is half your project
  - Probably the more difficult half to debug
  - From here on we'll work on motion estimation

Checkpoint 3 (2)

Async FIFO (1)
- Similar to a previous labs
- FIFO is 32bits x 255lines
- In and out ports are clocked separately
- These are very hard to make!
  - Why?
  - COUNTERS!!
Async FIFO (2)
- How full is your Async FIFO?
  - Just count reads and writes
  - Why is this complicated?
  - How big are these counters?
  - Remember Problem Set #6?

You need a multi-bit counter to cross a clock boundary! Major synchronization problems!

Async FIFO (3)
- FIFO must never be empty or full
  - Full -> You will lose data
  - Empty -> You will create garbage data
- How do we know when to write?
  - Check “wr_count”
- How do we know when to read?
  - Why don’t we give you “rd_count” too?

Sync FIFO (1)
- Almost Identical
- FIFO is 32bits x 256 lines
- FIFO must never be empty or full
  - Full -> You will lose data
  - Empty -> You will create garbage data
- How do we know when to read?
  - Check “data_count”
  - Why is there only one counter this time?

FIFO Sizing (1)
- Why do we give one with 32bits?
  - A) Video Decoder has 32bit output?
  - B) Block Motion Estimator will require this?
  - C) SDRAM has 32bit input?
  - D) Both A&C
  - E) We’re just messing with you...

C! Why not A/D though?

FIFO Sizing (2)
- Why 32x 256/255 Lines?
  - (NOTE: Asyncs are always a little smaller)
  - A) We wanted to make it really deep, to make life easier for you
  - B) Making it smaller is pointless
  - C) We wanted to make it big enough to store a full line of video

B! But Why?
BlockRAM Size is 4096bits

FIFOs (1)
FIFOs (2)

- DO NOT MODIFY THE FIFOs!!!
- Any changes you make may prevent them from simulating/synthesizing
- We gave you them the way we wanted you to use them
- If you think you HAVE to modify them, talk to us, something is wrong...
- Questions?

Announcements (1)

- Checkpoint2 Due Today @ 4pm
  - We will post our encoder at 4pm sharp
  - You may checkoff through Tuesday for 75% credit
- Checkpoint3 Due Tuesday 11/4
  - Check off sheets will be posted
  - This one will be tricky if you had trouble with checkpoints 1 or 2
- Checkpoint4 Due Friday 11/7
  - It will be TRIVIAL

Announcements (2)

- Design Reviews
  - Saw some great block diagrams
  - We need to collect a copy of them!
  - A lot of people neglected time/bandwidth
  - Calculate EVERYTHING!
    - Memory Requirements
    - Time (Can you design even run at 27MHz)
    - Bandwidth
    - Chip Resources (Registers, BlockRAMs, LUTs?)

Announcements (3)

- Design review schedule
  - We want ASMDs this week
  - RTL/ASMD/Verilog next week!
- BRING PHOTOCOPIES
  - If you hand it in late you get 50%

SDRAM Changes (1)

- We don’t stop!
  - In checkpoint 1 we filled memory and stopped
  - Now we need to keep going
- Change the addressing
  - Instead of just counting we need a scheme that will work with our block motion estimator

SDRAM Changes (2)

- ...Addressing (continued)
  - What do we need?
  - Random Access to a specific line/pixel
  - HOW?
- Do not change SDRAM mode or burst widths
- How many frames should you store?
  - Think ahead!
**SDRAM Changes (3)**
- No PN Generators
- You have a time budget now!
- If the FIFOs are full or empty YOU WILL NOT BE ABLE TO GET A WORKING CHECKPOINT 3
- Questions about SDRAM?

**BlockSelectRAM+ (1)**
- 4096 bits each
- Two complete read/write ports
- These are totally independent
- You can read/write on two different clocks
- A big part of the Async FIFOs!
- Data/Address Width is Variable
  - Data Width * 2^Address Width = 4096 bits

**BlockSelectRAM+ (2)**
- We have 160 BlockRAMs
- Is this enough to store a frame or field?
  - 320x240x8/4096 = 614400/4096 = 150
- Barely enough, for a single field
- This would KILL our routing

**Simulation Notes (1)**
- Checkpoint2 FIFOs were an old version
  - Sorry about that
- To simulate the FIFOs you must add libraries to your ModelSim simulation
  - C:\ModelTech_5.7d\Xilinx\Verilog\...
  - Unisims
  - Simprims
  - XilinxCore

**Simulation Notes (2)**
- Some of the libraries have problems
  - Remember gbl.GRST from the early labs?
  - Copy the library files you need to a directory that's part of your project
  - Comment out the gbl.GRST lines and the similarly suspicious ones
  - OR:
    - Use Black.V and Util.V where possible (you'll still need to copy files from the libraries)

**Simulation Notes (3)**
- Some of these labs are completely new
- ModelSim is a newer version than the last time we used the old labs
- Watch the website for file updates
  - Please read the newsgroup too
- We'll try to find a better way to get the simulation libraries set up
Where to Start

- Follow the data path
  - Decoder, FIFO, SDRAM, FIFO, Encoder
- Read the Verilog
  - FPGA_TOP.V (Blank)
  - SDRAM_TOP/SDRAM_CNTRL
  - The FIFO datasheets (Given)
  - With some thinking!

And now...

- We will check off Checkpoint2
  - You have till 4pm to be checked off
  - Its due today (75% credit till tuesday)
- Questions?
  - Stick around and ask
  - Stick around and listen, you might hear something very useful.