Lab Lecture 13
Project Report
11/21/2003

Due Dates
- Thr 11/20 @ 11am: Group Name
  - If you missed it see me after lab lecture
- Fri 11/21 @10am: Early Checkoff Files
- Wed 11/26 @ 10am: Checkoff Files
  - You may only submit *.V and *.EDN files
  - NO BITFILES OR PROJECTS
- Fri 12/5 @ 4pm: Final Project Report
  - And partner evaluation

Checkoff Procedures (1)
- You must sign up for a group name
  - Submit your *.V and *.EDN files
  - \fileservice\cs150\cs150\2003Fall\[Your Group Name]
- Make sure you submitted files will compile
  - We will constrain the clock to 27MHz

Checkoff Procedures (2)
- Sign up for a Checkoff Slot
  - You can change up till checkoff time
  - Early slots are better, we'll be nicer
  - ALL FILES DUE BY 10AM!
- Show up at LEAST 20min early
- Sign up for a X:00, X:20 or X:40 slot
  unless they're all full

Checkoff Procedures (3)
- We’ll compile files ahead of time
  - You'll want to be there if things break
- BOTH YOU AND YOUR PARTNER MUST BE PRESENT!
  - We need to talk to you both
- We will test your project
- We will ask you questions
Project Report (1)
- Look at the Report Spec
- Make sure to use our title page
- You should separately fill out partner evaluations
- You will get your project report and grade at the end of the final exam

Project Report (2)
- Typed and properly formatted
- Minimum 12pt with 1 inch margins
- Max 9 pages of text, 20 pages with diagrams
- Label all figures clearly
- Use useful signal names
- Be concise

Project Report (3)
- Document Project Functionality
  - Features
  - Inputs
- Technical Descriptions
  - Don’t repeat the assignment
  - Superficial information on most modules
- Detailed description of BME
  - This should be the core of your report

Project Report (4)
- BME (and Encoder)
  - Accurate and detailed
  - Lots of figures
  - These are the parts unique to each group
- Other Components
  - Give a reasonable description
  - We already know how most things work

Project Report (5)
- Purpose and Design
  - What did you do?
  - Why did you do it?
  - What did you change later?
  - How does it work?
  - What bugs did you fix?

Project Report (6)
- Diagrams
  - Must be clearly labeled
  - Use descriptive signal names
  - DO NOT COPY OUR DIAGRAMS
- State Diagrams/ASMDs
  - Use useful state names
  - Use mnemonic labeling not binary
Project Report (7)

- Submit to fileservice
  - Same place as your project
  - Electronic version MAY BE INCOMPLETE
  - We will not grade this, we just want a copy
- Hand in paper copy in the lab
  - There will be a TA there most of the day
- Reports are by Fri 12/5 by 4pm

Project Grading

- Checkoff
  - Tests
  - Questions
  - Extra Credit
- Report
  - Clarity
  - Usefulness
  - Verilog
  - Is your verilog readable?

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