Recap: 9/7 → 9/12

1. Verilog
   (a) General
      i. module, input, output
      ii. wire
      iii. reg
      iv. Bus notation [x:y]
      v. localparam
      vi. .Port(Wire) notation
   (b) Structural
      i. Primitive Gates: and, or, not, xor, nand, nor, xnor
      ii. Module instantiation
   (c) Behavioral
      i. assign
      ii. always@(posedge Clock)
      iii. always@( * )
      iv. <= (non-blocking statements)
      v. = (blocking statements)
      vi. (...) ? ... : ...; (ternary statements)
      vii. case vs. casex
         • default

2. Finite State Machines
   (a) Mealy vs. Moore machines
   (b) Verilog Implementation
      i. Module wrapper
      ii. State Encoding
      iii. Storing current state
      iv. State transitions
      v. Output
   (c) FSM communication to outside units

3. Sequential Logic Elements
   (a) Shift Register
   (b) Counters
      i. Binary Counter
      ii. Standard up-Counter