Name: _________________________________ ID#: ____________

- There are 6 problems worth 100 points total. There is little room for partial credit—it's better to do half the test carefully than to do the entire test sloppily.

<table>
<thead>
<tr>
<th>Problem</th>
<th>Points</th>
<th>Your Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td></td>
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<td>3</td>
<td>25</td>
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</tr>
<tr>
<td>4</td>
<td>28</td>
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</tr>
<tr>
<td>5</td>
<td>15</td>
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</tr>
<tr>
<td>6</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100</strong></td>
<td><strong>100</strong></td>
</tr>
</tbody>
</table>

In the real world, unethical actions by engineers can cost money, careers, and lives. The penalty for unethical actions on this exam will be a grade of F in EECS150 and a letter will be written to the Department Chair and to the Office of Student Conduct.
Problem 1  (14 points)

[4 pts.] a) Find the minimal sum-of-products form for $Y = \sum (3, 6, 7, 8, 9, 10, 11, 15)$ using variables $A_3A_2A_1A_0$. (For example, minterm 3 = $A_3\bar{A}_2A_1A_0$.)

$Y = \quad$ 

[4 pts.] b) Find the minimal product-of-sums form for $Y = \sum (3, 6, 7, 8, 9, 10, 11, 15)$ using variables $A_3A_2A_1A_0$. (For example, minterm 3 = $A_3\bar{A}_2A_1A_0$.)

$Y = \quad$ 

[6 pts.] c) State minimization. For the following state table, determine which states are equivalent.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Input</th>
<th>Output</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>0</td>
<td>0</td>
<td>S0</td>
</tr>
<tr>
<td>S0</td>
<td>1</td>
<td>0</td>
<td>S1</td>
</tr>
<tr>
<td>S1</td>
<td>0</td>
<td>1</td>
<td>S0</td>
</tr>
<tr>
<td>S1</td>
<td>1</td>
<td>1</td>
<td>S1</td>
</tr>
<tr>
<td>S2</td>
<td>0</td>
<td>0</td>
<td>S2</td>
</tr>
<tr>
<td>S2</td>
<td>1</td>
<td>0</td>
<td>S3</td>
</tr>
<tr>
<td>S3</td>
<td>0</td>
<td>1</td>
<td>S2</td>
</tr>
<tr>
<td>S3</td>
<td>1</td>
<td>1</td>
<td>S3</td>
</tr>
<tr>
<td>S4</td>
<td>0</td>
<td>0</td>
<td>S2</td>
</tr>
<tr>
<td>S4</td>
<td>1</td>
<td>0</td>
<td>S0</td>
</tr>
<tr>
<td>S5</td>
<td>0</td>
<td>0</td>
<td>S0</td>
</tr>
<tr>
<td>S5</td>
<td>1</td>
<td>0</td>
<td>S2</td>
</tr>
<tr>
<td>S6</td>
<td>0</td>
<td>0</td>
<td>S4</td>
</tr>
<tr>
<td>S6</td>
<td>1</td>
<td>0</td>
<td>S5</td>
</tr>
</tbody>
</table>
Problem 2  (6 points)

You are given a 200-meter length of cable with impedance 50 ohms and propagation velocity $2 \times 10^8$ m/s. The source end is driven with a 0-ohm impedance. The load end is open circuited. An oscilloscope probe (with 10-meg ohm input impedance) is connected to the cable 100 meters from the source, as shown below:

$V_0$ switches at time $t = 0$, as shown. Sketch the voltage seen on the oscilloscope for $0 < t < 10\mu s$. ($V_0$ is initially at 5V, $-\infty < t < 0$.)
Problem 3  Serial LED PWM Display (25 points)

In this problem, you will design the data path and controller state diagram for a 16-element LED display. The brightness of each LED is controlled by its duty cycle (using pulse width modulation), which is specified by a 4-bit value (0/15, 1/15, 2/15, ..., 15/15) stored in a 16×4 RAM. All components are driven by a 10MHz system clock. The data (on/off for each LED) is shifted into the display shift register in 1.6\( \mu \)s, then displayed for 24.0\( \mu \)s.

[11 pts.] a) Complete a detailed block diagram of the data path for the LED PWM Display, using up to three CB4RE synchronous binary counters, one COMPM4 4-bit magnitude comparator, and one COMP4 identity comparator. Note that CB4RE has both a TC output = \( Q_3 \cdot Q_2 \cdot Q_1 \cdot Q_0 \) and CEO = \( TC \cdot CE \). Also, SR4RE shifts left.
Problem 3 (cont.)

[1 pts.] b) List the input signals to the data path that come from the control FSM.

[1 pts.] c) List the output signals from the data path that are inputs to the control FSM.

[10 pts.] d) Draw (a) state diagram(s) for a control FSM that will continuously turn on each LED for a fraction of time proportional to the value of its corresponding RAM location. (For example, if address 3 has contents 8, then LED3 should be on 8/15 of the display enable time.) Do not use more than 3 states. Ensure that FSM and data path start correctly.

[2 pts.] e) Why does the clock to the shift register need to be as fast as possible?
Problem 4  (28 points)

Using the data path on page 11, determine the appropriate timing diagram from page 9, and list in register transfer notation the operation(s) that is (are) occurring at the rising edge of the clock. Also, note where any bus conflicts occur. For clock edge 1.5, 2.5, 3.5, etc., list in RTN the operation occurring at the falling edge.

Consider that the FSM outputs may have glitches unless de-glitching flip flops are used. The notation for outputs is as follows: SIG output directly from FSM may have glitches, SIG↑ is passed through a rising edge-triggered DFF that generates a clean SIG, and SIG↓ is passed through a falling edge-triggered DFF that generates a clean SIG.

Assume that the clock is slow, say 1 MHz, but that outputs may be delayed from 0 to 100 ns because of routing delays. A BUFGS is used to prevent clock skew.

On clock edge 0, the FSM enters state S0; on clock edge 1, the FSM enters state S1, etc.

Assume that signals that are tied to “0” or “1” are glitch free. Assume worst case timing for register transfer operations.

Recall that WE over-rides OE for the static RAM in the data path. For all state diagrams, ALU operation is Y=B (ALU[1:0]=01). For RTN descriptions, assume worst case possibility.
Problem 4 (cont.) – Data paths

a. Reset

OE = 1, IRLOAD = 0

Are bus conflicts possible?

If yes, state where they occur:

b. Reset

OE = 1, IRLOAD = 0

Are bus conflicts possible?

If yes, state where they occur:

c. IRLOAD = 0

Are bus conflicts possible?

If yes, state where they occur:
Problem 4 – Data paths (cont.)

d.

Reset

\[
\begin{array}{c}
S0 \quad \text{IRLOAD} = 0, \text{OE} = 1 \\
S1 \quad \text{IROUT} \uparrow \\
S2 \quad \text{IROUT} \uparrow \\
S3 \quad \text{CS} \downarrow \\
S4 \quad \text{MBRLOAD} \\
\end{array}
\]

\[
\begin{array}{c}
\text{IROUT} \uparrow \\
\text{WE} \uparrow \\
\text{CS} \downarrow \\
\text{WE} \uparrow \\
\text{RBUSOUT} \uparrow \\
\end{array}
\]

timing diagram (from page 9)

Are bus conflicts possible?
If yes, state where they occur:

- Clock edge 1: __________________________
- Clock edge 1.5: _________________________
- Clock edge 2: __________________________
- Clock edge 2.5: _________________________
- Clock edge 3: __________________________
- Clock edge 4: __________________________

e.

Reset

\[
\begin{array}{c}
S0 \quad \text{CS} = 1, \text{IRLOAD} = 0 \\
S1 \quad \text{WE} \downarrow \\
S2 \quad \text{RBUSOUT} \\
S3 \quad \text{MBRLOAD} \\
S4 \quad \text{OE} \downarrow \\
\end{array}
\]

\[
\begin{array}{c}
\text{IO} \uparrow \\
\text{ROUT} \\
\end{array}
\]

Are bus conflicts possible?
If yes, state where they occur:

- Clock edge 1: __________________________
- Clock edge 1.5: _________________________
- Clock edge 2: __________________________
- Clock edge 2.5: _________________________
- Clock edge 3: __________________________
- Clock edge 4: __________________________

f.

Reset

\[
\begin{array}{c}
S0 \quad \text{OE} = 1, \text{IRLOAD} = 0 \\
S1 \quad \text{IROUT} \uparrow \\
S2 \quad \text{WE} \uparrow \\
S3 \quad \text{RBUSOUT} \uparrow \\
S4 \\
\end{array}
\]

\[
\begin{array}{c}
\text{CS} \downarrow \\
\text{IROUT} \uparrow \\
\text{CS} \downarrow \\
\text{IROUT} \uparrow \\
\end{array}
\]

Are bus conflicts possible?
If yes, state where they occur:

- Clock edge 1: __________________________
- Clock edge 1.5: _________________________
- Clock edge 2: __________________________
- Clock edge 2.5: _________________________
- Clock edge 3: __________________________
- Clock edge 4: __________________________
Problem 4 – Data paths (cont.)

g.

Are bus conflicts possible?
If yes, state where they occur:

<table>
<thead>
<tr>
<th>Clock Edge</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

Timing diagram (from page 9)
Problem 5  (15 points)

[12 pts.] a) Using the data path on page 11 and microprogrammed controller on page 12, write a microprogram, in symbolic form, to execute the following register transfer operations in the order listed:

<table>
<thead>
<tr>
<th>RTN</th>
<th>Microcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) RAM[IR] → MBR</td>
<td></td>
</tr>
<tr>
<td>2) RAM[PC] → IR</td>
<td></td>
</tr>
<tr>
<td>3) MBR → RAM[IR]</td>
<td></td>
</tr>
<tr>
<td>4) PC+1 → PC</td>
<td></td>
</tr>
</tbody>
</table>

[3 pts.] b) Assuming the RTN in part (a) represents the execute portion of an instruction cycle, state in a sentence what assembly language instruction is being executed, e.g., ADD or LOAD or BRN or DJNZ or ?. (Assume the PC has already been incremented after the instruction fetch.)
Problem 5 (cont.) – Data path

16Kx16 RAM
address
Data IO

ALU op
00 Y=A
01 Y=B
10 Y=A plus B
11 Y=A minus 1

DataBus

OE L WE L CS L
OE WE CS

AC<15>

ACLOAD

load
D Q
AC

clock

ALU1 ALU0

Y

B 1 0

load
D Q
MBR

clock

MBRLOAD

load
D Q

RBUS

IR<15:14>

load
D Q
IR

clock

IRLOAD

IROUT

CLRPC

PCLOAD

PC+1

cnt

load

D Q
PC

clock

clock

load

D Q

11 Y=A minus 1

00 Y=A
01 Y=B

Data IO

ABUS
Problem 6  FSM Microprogram Analysis (12 points)

Consider the given FSM: Each FF has setup time $t_{su}$, hold time $t_{hld}$, for D and CE inputs. Propagation delay for each FF is $\geq t_{ckoMIN}$ and $\leq t_{ckoMAX}$. Inverter delay is $T_{INV}$. $t_{su}$ and $t_{hld}$ are less than 10 ns.

[2 pts.] a) Assuming proper operation, draw the state diagram for the FSM, assuming $T_3 = T_4 = 0$ ns. Use notation for the state as $Q_1 Q_0$. 

[1 pt.] b) Calculate the minimum clock period $T_{clkMIN}$. 

[2 pts.] c) Calculate the maximum clock period $T_{clkMAX}$. 

[2 pts.] d) Calculate the maximum response time $T_{respMAX}$. 

[1 pt.] e) Calculate the minimum response time $T_{respMIN}$. 

[1 pt.] f) Calculate the maximum clock frequency $f_{clkMAX}$. 

[1 pt.] g) Calculate the minimum clock frequency $f_{clkMIN}$. 

[2 pts.] h) If $T_{clkMIN}$ is greater than the clock cycle time, what should be done? 

[1 pt.] i) What is the critical path? 

[1 pt.] j) What is the critical delay? 

[2 pts.] k) Sketch a timing diagram for the FSM.
Problem 6 (cont.)

[2 pts.] b) With ENABLE = 1, $T_3 = T_4 = 0$ ns, what is the minimum clock period? (Express algebraically.)

\[
\text{period} \geq \boxed{} 
\]

[2 pts.] c) With $T_3 = T_4 = T_5 = 0$ ns, $T_6 = 50$ ns, and clock period = 100 ns, an asynchronous input ENABLE lasting 50 ns is input to the FSM. Estimate the chance of violating a setup or hold time on either FF, assuming uniform distribution of the ENABLE input change.

\[
\text{chance of violation:} \boxed{} 
\]

[3 pts.] d) With $T_3 = T_5 = T_6 = 0$, and ENABLE = 1, what is the maximum $T_4$ for proper operation of the FSM?

\[
T_4 \leq \boxed{} 
\]

[3 pts.] e) With $T_4 = T_5 = T_6 = 0$, and ENABLE = 1, what is the maximum $T_3$ for proper operation of the FSM?

\[
T_3 \leq \boxed{} 
\]