CMOS Inverters:

**Fig. 1 (a) CMOS inverter circuit. (b) Schematic transfer characteristics showing five regions of operations.**

<table>
<thead>
<tr>
<th>Region</th>
<th>$v_I$</th>
<th>$v_O$</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$v_I &lt; V_{TN}$</td>
<td>$V_H \sim V_{DD}$</td>
<td>Cutoff</td>
<td>Triode</td>
</tr>
<tr>
<td>2</td>
<td>$V_{TN} &lt; v_I &lt; v_O -</td>
<td>V_{TP}</td>
<td>$</td>
<td>High</td>
</tr>
<tr>
<td>3</td>
<td>$v_O -</td>
<td>V_{TP}</td>
<td>&lt; v_I &lt; v_O + V_{TN}$</td>
<td>$\sim V_{DD}/2$ **</td>
</tr>
<tr>
<td>4</td>
<td>$v_O + V_{TN} &lt; v_I &lt; V_{DD} -</td>
<td>V_{TP}</td>
<td>$</td>
<td>Low</td>
</tr>
<tr>
<td>5</td>
<td>$V_{DD} -</td>
<td>V_{TP}</td>
<td>&lt; v_I$</td>
<td>$V_L \sim 0$</td>
</tr>
</tbody>
</table>

* Note: $V_{TP}$ is usually a negative number.

** $v_O$ changes rapidly with $v_I$ in Region 3, the precise value depends on the slope of their i-v curves in the saturation region.

Figure 1 shows the circuit diagram and the schematic transfer characteristics of a CMOS inverter. (Please ignore the voltage scale in the transfer curve. It was obtained with $V_{DD} = 2.5$ V. We will be using 5V and different transistors). There are five regions of operation, as shown in Table 1. To calculate the theoretical transfer curve, you need to use the equations corresponding to the operation regions of NMOS and PMOS, respectively. For example, in Region 2,

$$i_{D,NMOS} = \frac{K_n}{2} (v_{GS,N}-V_{TN})^2 = \frac{K_n}{2} (v_I-V_{TN})^2$$

$$i_{D,PMOS} = K_p \left( |v_{GS,P}| - |V_{TP}| - \frac{|V_{DS,P}|}{2} \right) |V_{DS,P}| = K_p \left( |V_{DD}-V_I| - |V_{TP}| - \frac{|V_{DD}-V_O|}{2} \right) (V_{DD}-V_O)$$

Since $i_{D,NMOS} = i_{D,PMOS}$, we can solve $v_O$ as a function of $v_I$. After you solve $v_O$, you should verify that indeed NMOS is in saturation and PMOS is in triode regime (by comparing $v_{DS}$ and $v_{GS} - V_{TN(P)}$).

Likewise, in Region 4, NMOS is in triode and PMOS is in saturation:
\[ i_{D,NMOS} = K_n \left( v_{GS,N} - V_{TN} - \frac{v_{DS,N}}{2} \right) v_{DS,N} = K_n \left( v_I - V_{TN} - \frac{v_O}{2} \right) v_O \]

\[ i_{D,PMOS} = \frac{K_p}{2} \left( |v_{GS,P}| - |V_{TP}| \right)^2 = \frac{K_p}{2} \left( v_{DD} - v_I - |V_{TP}| \right)^2 \]

Solve \( v_O \) as a function of \( v_I \) again and verify that operation regimes of NMOS and PMOS.

In Region 3, both NMOS and PMOS are in saturation region. To precisely determine \( v_O \), you will need to include the channel length modulation parameters for both NMOS and PMOS:

\[ i_{D,NMOS} = \frac{K_n}{2} \left( v_I - V_{TN} \right)^2 \left( 1 + \lambda_N v_O \right) \]

\[ i_{D,PMOS} = \frac{K_p}{2} \left( v_{DD} - v_I - |V_{TP}| \right)^2 \left( 1 + \lambda_P (V_{DD} - v_O) \right) \]

**PreLab Question:**

(Due to shortness of time, you are not required to turn in your Prelab before your Lab session. But you are highly encouraged to finish the Prelab before your Lab session. You will need this for your Lab Report, and you will be better off knowing how far your experimental and theoretical results while you are doing the experiments).

1. List the device parameters you have measured for your NMOS and PMOS. NMOS is from Lab 2, PMOS are from the first part of Lab 3):
   - \( V_{TN} = \) __________
   - \( K_n = \) __________
   - \( \lambda_N = \) __________ (Please include units in your list).
   - \( V_{TP} = \) __________
   - \( K_p = \) __________
   - \( \lambda_P = \) __________

2. Solve the transfer curves in Region 2, 3, and 4 using the formulation above. Obtain analytical solutions. To simply your expression, you can use the parameter \( K_r = \frac{K_n}{K_p} \)

3. Plug in the values of your device parameters; plot the transfer curve for \( v_I \) from 0 to 5V (\( V_{DD} \)).