1. Use inspection analysis to write an expression for the gain $v_{out}/v_{in}$ for each of the amplifiers in Fig. PS7.1. The expression should be in terms of the small signal equivalent circuits (i.e., $g_m$, $g_{mb}$, $r_x$, $r_o$, $\beta$, etc.) for the transistors used. Assume the transistors are matched and neglect the parasitic capacitances of transistors.

![Fig. PS7.1](image.png)

2. For the BJT differential amplifier shown in Fig. PS7.2, assume $V_T = 25\text{mV}$ and $V_A \to \infty$:
   (a) Write an expression in terms of $(I_{TAIL}R_C)$ for the differential gain.
   (b) Write an expression for the maximum permitted value for the input common mode voltage $V_{CM}$ while the transistors remain comfortably in the active region with their collector voltages not lower than their base voltages (i.e., $V_{CB} \geq 0$). Express this maximum in terms of $V_{CC}$ and the differential gain obtained in (a) and hence show that for a given value of $V_{CC}$, the higher the gain achieved, the lower the input common-mode range.
   (c) Assume $R_C = 5\text{k}\Omega$, $R_{TAIL} = 1\text{M}\Omega$, and $I_{TAIL} = 1\text{mA}$. Suppose two small signals are fed to the bases of the two input transistors with $v_{i1} = 2v_{i2} = 5\text{mV}$. Calculate the output common mode voltage $v_{oc}$, and differential output voltage $v_{od}$.
   (d) Assuming $I_{TAIL} = 0$ (i.e., only $R_{TAIL}$ exists) and $\beta = 200$, select values of $R_C$ and $R_{TAIL}$ to give a differential input resistance of $2\text{M}\Omega$, a differential voltage gain of 500, and a CMRR of 500.
   (e) Assume the $\beta$s of two transistors are $\beta_1$ and $\beta_2$ and everything else is matched. Show that the input offset voltage is approximately $V_T \times |(1/\beta_1) - (1/\beta_2)|$.
   (f) Assume the collector load resistors $R_C$ and the scale currents $I_S$ of the transistors are mismatched by 10%. Calculate the input offset voltage.
(g) Suppose a design error has resulted in a gross mismatch in the circuit where \( Q_1 \) has an emitter-base junction area twice that of \( Q_2 \). Assuming the input signal is a small differential signal, express \( I_{C1} \) and \( I_{C2} \) in terms of \( I_{\text{TAIL}} \).

(h) Continuing from (g), if \( R_C = 5k \Omega \), \( R_{\text{TAIL}} = 1M \Omega \) and \( I_{\text{T A I L}} = 1mA \), calculate \( A_{cm} \), \( A_{cm-dm} \), and \( A_{dm} \). Assume \( \beta \) is very large.

![Fig. PS7.2](attachment:fig-ps7-2.png)

3. The op amp in the circuit of Fig. PS7.3 has an open-loop gain of 10,000, an offset voltage of 1mV, and an input-bias current of 100nA.

(a) What is the output voltage if the op amp is ideal?

(b) What is the actual output voltage for the worst-case polarity of offset voltage?

(c) What is the worst-case percentage error in the output voltage compared to the ideal output voltage?

(d) Assuming the op amp has a finite 3dB frequency of 100 kHz, estimate the closed loop 3dB frequency.

![Fig. PS7.3](attachment:fig-ps7-3.png)
4. For the differential amplifier with current mirror load shown in Fig. PS7.4(a), assume all transistors have the same $k'W/L = 3.2 \text{ mA/V}^2$, and $\lambda = 0.05$. Neglect body effect.

(a) Find the required bias current $I$ for a gain $v_o/v_{id} = 80 \text{ V/V}$ for the circuit in Fig. PS7.4(a).

(b) Suppose the ideal current source is implemented in two cases: (1) a simple current mirror as shown in Fig. PS7.4(b); (2) a cascade current mirror as shown in Fig. PS7.4(c). Assume $I_{REF}$ is adjusted to the bias current obtained in part (a). Find the CMRR for both cases.

Fig. PS7.4