EE247
Lecture 11

• Switched-Capacitor Filters (continued)
  – Effect of non-idealities
  – Bilinear switched-capacitor filters
  – Filter design summary
• Comparison of various filter topologies
• Data Converters

Summary
Last Lecture

• Switched-capacitor filter design considerations
  – DDI & LDI Integrator characteristics
  – Bottom-plate LDI integrator → overcomes parasitic sensitivity issues
  – Continuous-time and complex conjugate terminations
  – Use of T-networks to implement high capacitor ratios
• Switched-capacitor filters utilizing
Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

Assumption-

Opamp → does not slew (will be revisited)
Opamp has only one pole → exponential settling


\[ H_{\text{actual}}(Z) = H_{\text{ideal}}(Z) \left[ 1 - e^{-k} + e^{-k} \times \frac{C_I}{C_I + C_s} z^{-1} \right] \]

where \( k = \pi \times \frac{C_I}{C_I + C_s} \times \frac{f_t}{f_s} \)

\( f_t \to \text{Opamp unity-gain-frequency} \), \( f_s \to \text{Clock frequency} \)

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

Magnitude deviation due to finite opamp unity-gain-frequency

Example: 2nd order bandpass with Q=25

Effect of Opamp Finite Bandwidth
Maximum Achievable Q

Max. allowable
biquad Q for
peak gain
change <10%

Ref: K. Martin, A. Sedra, “Effect of the Opamp Finite Gain & Bandwidth on the Performance of

Example:
For Q of 40 required
Max. allowable biquad Q
for peak gain change <10%

1- \( f_c/f_s = 1/32 \)
   \( f_c/f_s - 0.02 \)
   \( f_t > 50f_c \)

2- \( f_c/f_s = 1/12 \)
   \( f_c/f_s - 0.035 \)
   \( f_t > 28f_c \)

3- \( f_c/f_s = 1/6 \)
   \( f_c/f_s - 0.05 \)
   \( f_t > 20f_c \)

Ref: K. Martin, A. Sedra, “Effect of the Opamp Finite Gain & Bandwidth on the Performance of
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Critical frequency deviation due to finite opamp unity-gain-frequency

Example: 2nd order filter

Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

- Cont. time termination (Q) implementation
- Folded-Cascode opamp with $f_o = 100\text{MHz}$ used
- Center freq. $3.1\text{MHz}$, filter $Q=55$
- Clock freq. $12.83\text{MHz}$ → effective oversampling ratio 8.27
- Measured dynamic range 46dB ($IM3=1\%$)


Sources of Distortion in Switched-Capacitor Filters

- Distortion induced by finite slew rate of the opamp
- Opamp output/input transfer function non-linearity
- Distortion incurred by finite setting time of the opamp
- Capacitor non-linearity
- Distortion due to switch clock feed-through and charge injection
What is Slewing?

Assume opamp is of a simple differential-pair class A transconductance type

Class A amplifiers where the maximum output current is limited to $I_{ss}$:

\[
V_{in} < -V_{max} \Rightarrow I_o = g_m V_{in}
\]
\[
V_{in} > +V_{max} \Rightarrow I_o = I_{max}
\]
What is Slewing?

If at the rising edge of $\phi_2$: $V_{cs} > V_{\max} \Rightarrow$ Output current constant $I_o = Iss/2 \Rightarrow$ Slewing

After $V_{cs}$ is discharged enough to have $V_{cs} < V_{\max} \Rightarrow$ Linear settling

Distortion Induced by Opamp Finite Slew Rate
Ideal Switched-Capacitor Integrator Output Waveform

- During $\phi_1$, the input voltage $V_{in}$ is applied to the capacitor $C_s$, and the output voltage $V_o$ is determined by $V_o = \frac{V_{in}}{C_s/C_I}$.
- During $\phi_2$, the switch connects $C_s$ to $C_I$, transferring charge from $C_s$ to $C_I$.

Slew Limited Switched-Capacitor Integrator Output Settling

- The output $V_o$ settles in two stages: slewing and linear settling.
- During slewing, the output voltage transitions rapidly.
- During linear settling, the output voltage approaches its final value with a smaller rate.

Clock:
- $\phi_1$: Active phase for input application.
- $\phi_2$: Active phase for charge transfer.

Input Voltage $V_{in}$ and Output Voltage $V_o$ are shown graphically, with $V_{cs}$ indicating the charge stored on $C_s$.
Distortion Induced by Finite Slew Rate of the Opamp

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)

For high-linearity need to have either high slew rate or non-slewing opamp

\[ HD_k = \frac{V_o}{S}\left(\frac{\sin(\omega_kT)}{\omega_kT}\right)^2 \]

\[ HD_3 = \frac{V_o}{S}\left(\frac{\sin(\omega_3T)}{\omega_3T}\right)^2 \]

Example:
Slew Related Harmonic Distortion

\[ HD_3 = \frac{V_o}{S_f T_s} \times \frac{8(\sin \alpha V / 2)^2}{T_s} \]

Switched-capacitor filter with 4kHz bandwidth, \( f_s = 128kHz \), \( S_f = 1V / \mu s \), \( V_o = 3V \)


Distortion Induced by Opamp Finite Slew Rate

Example

- \( V_o = 1V \)
- \( V_o = 2V \)

\[ HD_3 \ [\text{dB}] \]

\[ (\text{Slew-rate} / f_s) [V] \]
Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - Can reduce slew limited linearity by using an amplifier with a higher slew rate only for the last stage
  - Can reduce slew limited linearity by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario

At the instant \( C_s \) connects to input of opamp \( t=0^+ \)
- Opamp not yet active at \( t=0^+ \) due to finite opamp delay
- Feedforward path from input to output generates a voltage spike at the output spike magnitude function of \( C_I, C_L, C_s \)
- Spike increases slewing period
- Eventually, opamp becomes active & starts slewing
Sources of Noise in Switched-Capacitor Filters

- Opamp Noise
  - Thermal noise
  - 1/f (flicker) noise
- Thermal noise associated with the switching process (kT/C)
  - Same as continuous-time filters
- Precaution regarding aliasing of noise required
Other z domain Integrators
Example: Bilinear

- Bilinear integrator

\[ v_o(nT) = v_o(nT-T) + k [v_i(nT) + v_i(nT-T)] \]
\[ [1 - z^{-1}] v_o(z) = k [1 + z^{-1}] v_i(z) \]
\[ H(z) = \frac{v_o(z)}{v_i(z)} = k \frac{1 + z^{-1}}{1 - z^{-1}} \]

Bilinear Integrator

- Not implemented by “standard” SC integrators
- Synthesis:
  Biquads: direct coefficient comparison
Example: Bilinear S.C. integrator:

\[ H(Z) = - \frac{C_x}{C_I} \frac{1}{1-Z^{-1}} \times \frac{L}{1-Z^{-1}} = - \frac{C_x}{C_I} \frac{1}{1-e^{-j\omega T}} \]
\[ = \frac{C_x}{C_I} \frac{1}{j\omega T_s} \frac{\omega T_s}{\tan(\omega T_s/2)} \]

Ideal Integrator | Magnitude Error

No Phase Error! For signals at frequency < sampling freq., Magnitude error negligible

LDI & Bilinear Transformation

Frequency Warping

**LDI:**
\[
\frac{1}{s} \Rightarrow \frac{Z^{-1/2}}{1-Z^{-1}} = T_s \frac{1}{2j\sin \omega T_s/2}
\]
\[
s \Rightarrow \frac{2}{T_s} j\sin \omega T_s/2
\]

**Bilinear**
\[
\frac{1}{s} \Rightarrow \frac{1+Z^{-1}}{1-Z^{-1}} e^{-j\omega T} = T_s \frac{1}{2} \frac{1}{j\tan \omega T_s/2}
\]
\[
s \Rightarrow \frac{2}{T_s} j\tan \omega T_s/2
\]

Other z domain Integrators

Example: Bilinear

- Frequency translation

\[
\left|\frac{1}{s}\right|_{z=e^{2\pi f_s T}} = H_{SC}(z)|_{z=e^{2\pi f_s T}} = 1
\]

**Bilinear**

\[
f_{RC} = \frac{f_s}{\pi} \tan \left( \frac{\pi f_{SC}}{f_s} \right)
\]

**LDI**

\[
f_{SC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right)
\]
Bilinear Transform

\[ f_{RC} = \frac{f_s}{\pi} \tan \left( \pi \frac{f_{SC}}{f_s} \right) \]

- Entire \( j\omega \) axis maps onto the unit circle
- Mapping is nonlinear (tan distortion)

\[ f_{RC} \text{ vs } f_{SC} \]

Bilinear & LDI Transformation Frequency Warping

As long as \( f \ll f_s \) error negligible
"Bilinear" Bandpass

\[ f_s = 100\text{kHz} \]
\[ f_c = f_s / 8 \]
\[ Q = 10 \]

Matlab:

\[
H(z) = \frac{0.0378 z^2 - 0.0378}{z^2 - 1.362 z + 0.9244}
\]

zero at \( f_s / 2 \)

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Martin-Sedra Biquad

Periodic AC Analysis

\[
\begin{align*}
V_o &= \frac{K_1 z^2 + (-2K_1 + K_2 + K_3)z + (K_1 - K_2, K_3)}{z^2 + (-2 + K_1, K_2 + K_3)z + (1 - K_2, K_3)}
\end{align*}
\]

Magnitude Response

LDI vs Bilinear Transform

- **LDI transform:**
  - Realized by “standard” switched-capacitor integrators
  - Some high frequency zeros may get lost
  - Simple filter synthesis:
    - Replace RC integrators with SC integrators
    - Ensure clock phases chosen so that all integrators loops LDI type
- **Bilinear transform**
  - Not implemented by “standard” SC integrators
  - Synthesis:
    - Biquads: direct coefficient comparison
    - Ladders: see
Switched-Capacitor Filter Application
Example: Voice-Band Codec (Coder-Decoder) Chip

CODEC Transmit Path

Highpass Filter

Note: $f_s = 8$ kHz

Low Q bandpass ($Q < 1$) filter shape → Implemented with lowpass followed by highpass
CODEC Transmit Path
Clocking Scheme

First filter (1st order RC type) performs anti-aliasing for the next S.C. biquad

The first 2 stage filters form 3rd order elliptic with corner frequency @ 32kHz → Anti-aliasing for the next lowpass filter

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency → Ease of anti-aliasing

SC Filter Summary

✓ Pole and zero frequencies proportional to
  – Sampling frequency $f_s$
  – Capacitor ratios
    ✔ High accuracy and stability in response
    ✔ Long time constants realizable without large $R$, $C$

✓ Compatible with transconductance amplifiers
  – Reduced circuit complexity, power dissipation

✓ Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)

🙏 Issue: Sampled-data filters → require anti-aliasing prefiltering
Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects:

- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Opamp finite slew rate
- Clock feedthru
- Switch+ sampling cap. finite time-constant

\[ \text{Magnitude Error} \]

\[ 5-10\text{MHz} \]

\[ \text{Filter bandwidth} \]

\[ \text{Assuming constant opamp } f_u \]

\[ \rightarrow \text{Limited switched-capacitor filter performance frequency range} \]

Summary
Filter Performance versus Filter Topology

<table>
<thead>
<tr>
<th>Filter Type</th>
<th>Max. Usable Bandwidth</th>
<th>SNDR</th>
<th>Freq. tolerance w/o tuning</th>
<th>Freq. tolerance + tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamp-RC</td>
<td>~10MHz</td>
<td>60-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-C</td>
<td>~5MHz</td>
<td>40-60dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-RC</td>
<td>~5MHz</td>
<td>50-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Gm-C</td>
<td>~100MHz</td>
<td>40-70dB</td>
<td>+40-60%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Switched Capacitor</td>
<td>~10MHz</td>
<td>40-90dB</td>
<td>&lt;&lt;1%</td>
<td></td>
</tr>
</tbody>
</table>
Data Converters

Material Covered in EE247

- Filters
  - Continuous-time filters
    - Biquads & ladder type filters
    - Opamp-RC, Opamp-MOSFET-C, gm-C filters
    - Automatic frequency tuning
  - Switched capacitor (SC) filters
- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Pipeline ADCs,....
    - Oversampled converters
    - Self-calibration techniques
- Systems utilizing analog/digital interfaces
  - Wireline communication systems- ISDN, XDSL....
  - Wireless communication systems- Wireless LAN, Cellular telephone,....
  - Disk drive electronics
  - Fiber-optics systems
Data Converter Topics

• Basic Operation of Data Converters
  – Uniform sampling and reconstruction
  – Uniform amplitude quantization

• Characterization and Testing

• Common ADC/DAC Architectures

• Selected Topics in Converter Design
  – Practical Implementations
  – Desensitization to Analog Circuit Non-Idealities

• Figures of Merit and Performance Trends

Suggested Reference Texts


Example: Typical Cell Phone

Contains in integrated form:

- 4 Rx filters
- 4 Tx filters
- 4 Rx ADCs
- 4 Tx DACs
- 3 Auxiliary ADCs
- 8 Auxiliary DACs

Dual Standard, I/Q

Audio, Tx/Rx power control, Battery charge control, display, ...

Total: Filters $\rightarrow$ 8
        ADCs $\rightarrow$ 7
        DACs $\rightarrow$ 12
Data Converter Basics

- DSP is wonderful, but...
- Real world signals are analog:
  - Continuous time
  - Continuous amplitude
- DSP can only process:
  - Discrete time
  - Discrete amplitude
  → Need for data conversion from analog to digital and digital to analog

A/D & D/A Conversion

A/D Conversion
- Analog In
- Anti-alias Filtering
- Sampling
- Quantization
- Digital Filter
- Digital Coding
- Digital Out

D/A Conversion
- Digital In
- Digital Filter
- Digital Decoding
- DAC
- Analog Hold
- Reconstruction Filtering
- Analog Out
Data Converters

• Stand alone data converters
  – Used in variety of systems
  – Example: Analog Devices AD9235 12bit/ 65Ms/s ADC-
  Applications:
    • Ultrasound equipment
    • IF sampling in wireless receivers
    • Hand-held scopemeters
    • Low cost digital oscilloscopes

Data Converters

• Embedded data converters
  – Cost, reliability, and performance \(\rightarrow\) integration of
    data conversion interfaces along with DSPs
  – Main issues
    • Feasibility of integrating sensitive analog functions in a
      technology optimized for digital performance
    • Down scaling of supply voltage
    • Interference & spurious signal pick-up from on-chip digital
circuitry
    • Portable applications dictate low power consumption
D/A Converter Transfer Characteristics

- For an ideal digital-to-analog converter with uniform, binary digital encoding & a unipolar output range from 0 to $V_{FS}$

$$V_0 = V_{FS} \sum_{i=0}^{N} \frac{b_i}{2^i} = \Delta \sum_{i=0}^{N} b_i \times 2^{N-i} \quad , \quad b_i = 0 \text{ or } 1$$

where $N = \# \text{ of bits}$

$V_{FS} = \text{full scale output}$

$\Delta = \text{step size}$

$\Delta = \frac{V_{FS}}{2^N}$

Note: $V_0(b_i = 1, \text{all} i) = V_{FS} - \Delta$

$$= V_{FS} \left( 1 - \frac{1}{2^N} \right)$$

Example: $N = 3$

$V_0 = \Delta (b_1 \cdot 2^1 + b_2 \cdot 2^0 + b_3 \cdot 2^0)$

Ideal D/A Transfer Characteristic

- Ideal DAC introduces no error!
- One-to-one mapping from input to output

Ideal Response

Step Height (1 LSB = $\Delta$)

Digital Input Code

Analog Output

$V_{FS}$

$V_{FS}/2$

$V_{FS}/8$
A/D Converter Transfer Characteristic

- For an ideal analog-to-digital converter with uniform, binary digital encoding & a unipolar input range for 0 to $V_{FS}$

$$V_{FS} = \text{full scale output}$$
$$\Delta = \text{step size}$$
$$\Delta = \frac{V_{FS}}{2^m}$$

Note: $D(bi=1, all i) \rightarrow V_{FS} - \Delta \rightarrow V_{FS}\left(1 - \frac{1}{2^m}\right)$

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Ideal A/D Transfer Characteristic

- Ideal ADC introduces error
  -> (+1/2\Delta)
  \[\Delta = \frac{V_{FS}}{2^m}\]
  \[m = \# \text{ of bits}\]

- This error is called "quantization error"
Data Converter Performance Metrics

• Data Converters are typically characterized by static, time-domain, & frequency domain performance metrics:
  – Static
    • Monotonicity
    • Offset
    • Gain error
    • Differential nonlinearity (DNL)
    • Integral nonlinearity (INL)
  – Dynamic
    • Delay, settling time
    • Aperture uncertainty
    • Distortion- harmonic content
    • Signal-to-noise ratio (SNR), Signal-to-(noise+distortion) ratio (SNDR)
    • Idle channel noise
    • Dynamic range & spurious-free dynamic range (SFDR)

What is a discrete time signal?

- A signal that changes only at discrete time instances?
- A continuous time signal multiplied with a train of infinitely narrow unit pulses?
- A vector whose element indices correspond to discrete instances in time?
- All of the above?
Discrete Time Signals

- A sequence of numbers (or vector) with discrete index time instants
- Intermediate signal values not defined (not the same as equal to zero!)
- Mathematically convenient, non-physical
- We will use the term "sampled data" for related signals that occur in real, physical interface circuits

Typical Sampling Process

CT $\Rightarrow$ SD $\Rightarrow$ DT

Continuous Time

Sampled Data (e.g. T/H signal)

Clock

Discrete Time

Physical Signals

"Memory Content"
Uniform Sampling

- Samples spaced $T$ seconds in time
- Sampling Period $T \leftrightarrow$ Sampling Frequency $f_s=1/T$
- Problem: Multiple continuous time signals can yield exactly the same discrete time signal (aliasing)

Summary

Data Converters

- ADC/DACs need to *sample/reconstruct* to convert from continuous time to discrete time signals and back
- We distinguish between purely mathematical discrete time signals and "sampled data signals" that carry information in actual circuits
- Question: How do we ensure that sampling/reconstruction preserves information