DAC Converters (continued)
- Reconstruction filter
- DAC self calibration techniques
  - Current copiers
  - Dynamic element matching

ADC Converters
- Sampling
  - Sampling switch induced distortion
  - Sampling switch charge injection
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching

DAC Reconstruction Filter

- Need for and requirements depend on application

- Tasks:
  - Correct for sinc distortion
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Digital and SC filter possible only in combination with oversampling (signal bandwidth $B << f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band sinc amplitude droop associated with the inherent DAC ZOH function

DAC Implementation Examples

- Untrimmed segmented
- Current copiers:
- Dynamic element matching:
An 80-MHz 8-bit CMOS D/A Converter

Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance
Current-Switched DACs in CMOS

\[ I_j = k(V_{G_{Sj}} - V_{thj})^2 \]
\[ V_{G_{Sj}} = V_{G_{Sj}} - 4RI, \quad V_{G_{Sj}} = V_{G_{Sj}} - 7RI \]
\[ V_{G_{Sj}} = V_{G_{Sj}} - 9RI, \quad V_{G_{Sj}} = V_{G_{Sj}} - 10RI \]
\[ I_j = k(V_{G_{Sj}} - V_{thj})^2 = I_j \left(1 - \frac{4RI}{V_{G_{Sj}} - V_{thj}}\right)^2 \]

\[ R_{on} = \frac{2I_j}{V_{G_{Sj}} - V_{thj}} \]
\[ \rightarrow I_2 = I_1 \left(1 - \frac{4RI_{on}}{2}\right)^2 = I_1 \left(1 - 4RI_{on}\right) \]
\[ \rightarrow I_3 = I_1 \left(1 - \frac{7RI_{on}}{2}\right)^2 = I_1 \left(1 - 7RI_{on}\right) \]
\[ \rightarrow I_4 = I_1 \left(1 - \frac{9RI_{on}}{2}\right)^2 = I_1 \left(1 - 9RI_{on}\right) \]
\[ \rightarrow I_5 = I_1 \left(1 - \frac{10RI_{on}}{2}\right)^2 = I_1 \left(1 - 10RI_{on}\right) \]

**Example: 5 unit element current sources**

- Assumption: \( RI \) is small compared to transistor gate overdrive
  - Desirable to have \( g_m \) small

**Current-Switched DACs in CMOS**

Example: INL of 7 unit element DAC

- Example: 7 unit element current source DAC- assume \( g_m x R = 1/100 \)
  - If switching of current sources sequential (1-2-3-4-5-6-7)
    \( \rightarrow \) INL = +0.25LSB
  - If switching of current sources symmetrical (4-3-5-2-6-7)
    \( \rightarrow \) INL = +0.09, -0.058LSB

Example: 5 unit element current sources

- Assumption: \( RI \) is small compared to transistor gate overdrive
  - Desirable to have \( g_m \) small
Current-Switched DACs in CMOS

Example: DNL of 7 unit element DAC

Input

DNL [LSB]

Example: 7 unit element current source DAC- assume $g_m \times R = 1/100$
•If switching of current sources sequential (1-2-3-4-5-6-7)
  \( \Rightarrow \text{DNL}_{\text{max}} = +0.15\text{LSB} \)
•If switching of current sources symmetrical (4-3-5-2-6-7 )
  \( \Rightarrow \text{DNL} = +0.15\text{LSB} \)

More recent published DAC using symmetrical switching built in 0.35μm/3V analog/1.9V digital, area x10 smaller compared to previous example.
A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

16bit DAC (6-10)- MSB DAC uses calibrated current sources
Current Divider Accuracy

\[ I_d = \frac{I_{d1} + I_{d2}}{2} \]
\[ dI_d = \frac{I_{d1} - I_{d2}}{I_d} \]
\[ dI_d = 2 \frac{I_d}{V_{GS} - V_{th}} \left[ \frac{dW}{w} \right] + dV_h \]

Ideal Current Divider
Real Current Divider
M1 & M2 mismatched

Problem: Device mismatch could severely limit DAC accuracy
Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

(a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

During $\Phi_1$

\[
I_1^{(1)} = \frac{1}{2} I_o (1 + \Delta_I) \\
I_2^{(1)} = \frac{1}{2} I_o (1 - \Delta_I)
\]

During $\Phi_2$

\[
I_1^{(2)} = \frac{1}{2} I_o (1 - \Delta_I) \\
I_2^{(2)} = \frac{1}{2} I_o (1 + \Delta_I)
\]

\[
\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2} = \frac{I_o (1 - \Delta_I) + (1 + \Delta_I)}{2} = \frac{I_o}{2} \text{ for } \Delta_I \text{ small}
\]
Dynamic Element Matching

During $\Phi_1$

$$I_{1}^{(1)} = \frac{1}{2} I_o (1 + \Delta_i)$$
$$I_{1}^{(2)} = \frac{1}{2} I_o (1 - \Delta_i)$$

$$\langle I_i \rangle = \frac{I_{1}^{(1)} + I_{1}^{(2)}}{2} = \frac{I_o}{4} (1 + \Delta_i)(1 + \Delta_i)$$

During $\Phi_2$

$$I_{1}^{(3)} = \frac{1}{2} I_o (1 + \Delta_i)$$
$$I_{1}^{(4)} = \frac{1}{2} I_o (1 - \Delta_i)$$

$$\langle I_i \rangle = \frac{I_{1}^{(3)} + I_{1}^{(4)}}{2} = \frac{I_o}{4} (1 + \Delta_i)(1 + \Delta_i)$$

E.g. $\Delta_1 = \Delta_2 = 1\% \Rightarrow$ matching error is $(1\%)^2 = 0.01\%$
Summary
D/A Converter

- D/A architecture
  - Unit element – complexity proportional to $2^B$ - excellent DNL
  - Binary weighted- complexity proportional to $B$ - poor DNL
  - Segmented- unit element MSB($B_1$) + binary weighted LSB($B_2$) → complexity proportional $(2^{B_1}-1) + B_2$ – DNL compromise between the two

- Static performance
  - Component matching

- Dynamic performance
  - Glitches

- DAC improvement techniques
  - Symmetrical DAC element switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching

MOS Sampling Circuits
Re-Cap

• How can we build circuits that "sample"

Ideal Sampling

• In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage \( v_{IN} \) onto the capacitor \( C \)

• Not realizable!
Ideal T/H Sampling

- $V_{out}$ tracks input when switch is closed
- Grab exact value of $V_{in}$ when switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)

Continuous Time

T/H signal (SD Signal)

Clock

DT Signal
Practical Sampling

- Switch induced noise power $\rightarrow kT/C$
- Finite $R_{sw} \rightarrow$ limited bandwidth
- $R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection
- Clock jitter

$kT/C$ Noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$C \geq 12k_B T \left( \frac{2^n - 1}{V_{FS}} \right)^2$$

In high resolution ADCs $kT/C$ noise usually dominates overall error (power dissipation considerations).

<table>
<thead>
<tr>
<th>$B$</th>
<th>$C_{min} (V_{FS} = 1V)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
</tr>
<tr>
<td>14</td>
<td>13 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
</tr>
</tbody>
</table>
Acquisition Bandwidth

- The resistance $R$ of switch $S_1$ turns the sampling network into a lowpass filter with risetime $= RC = \tau$

- Assuming $V_{in}$ is constant during the sampling period and $C$ is initially discharged

\[ v_{out}(t) = v_{in} \left( 1 - e^{-t/\tau} \right) \]

Switch On-Resistance

\[ V_{in} - V_{out} \left( t = \frac{1}{2 f_s} \right) \ll \Delta \]

\[ V_{in} e^{-t/2 f_s} \ll \Delta \]

Worst Case: $V_{in} = V_{FS}$

\[ \tau \ll \frac{T}{2 \ln \left( 2^B - 1 \right)} \]

\[ R \ll \frac{1}{2 f_s C \ln \left( 2^B - 1 \right)} \]

Example:

$B = 14$, $C = 13 \text{pF}$, $f_s = 100 \text{MHz}$

$T/\tau \gg 19.4$, $R \ll 40 \Omega$
Switch On-Resistance

\[ I_{DS(min)} = \mu C_m \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \]

\[ \frac{1}{R_{ON}} \equiv \left. \frac{dI_{DS(min)}}{dV_{DS}} \right|_{V_{DS} \to 0} \]

\[ R_{ON} = \frac{1}{\mu C_m \frac{W}{L} (V_{GS} - V_{th})} = \frac{1}{\mu C_m \frac{W}{L} (V_{DD} - V_{th} - V_{in})} \]

for \( R_a = \frac{1}{\mu C_m \frac{W}{L} (V_{DD} - V_{th})} \)

\[ R_{ON} = \frac{R_a}{1 - \frac{V_{in}}{V_{DD} - V_{th}}} \]

---

Sampling Distortion

\[ V_{out} = V_{in} \left( 1 - e^{-\frac{F}{2\pi \left( \frac{V_{in}}{V_{DD} - V_{th}} \right)}} \right) \]

For 10-bit ADC & \( T/\tau = 10 \)

- DC: -35.1dBFS
- HD1: -41.0dBFS
- HD2: -41.4dBFS
- HD3: -77.7dBFS

\[ V_{DD} - V_{th} = 2V \quad V_{FS} = 1V \]
Sampling Distortion

- SFDR is very sensitive to sampling distortion
  
- Solutions:
  - Overdesign → Larger switches
  - Increased switch charge injection
  - Increased switch drain & source C
  - Complementary switch
  - Maximize \[ V_{DD}/V_{FS} \]
  - Decreased dynamic range
  - Constant \[ V_{GS} \] ? \( f(V_{in}) \)

Practical Sampling

- \( kT/C \) noise
  \[ C \geq 12kT \left( \frac{2^B - 1}{V_{FS}} \right)^2 \]

- Finite \( R_{sw} \) → limited bandwidth
  \[ R << \frac{1}{2f_i C \ln(2^B - 1)} \]

- \( g_{sw} = f(V_{in}) \) → distortion
  \[ g_{on} = g_{o} \left( 1 - \frac{V_{in}}{V_{DD} - V_{th}} \right) \quad \text{for} \quad g_{o} = \mu C_{in} \frac{W}{L} (V_{DD} - V_{th}) \]

- Switch charge injection
- Clock jitter
Sampling Distortion

Effect of Supply Voltage

- Effect of lower supply voltage on sampling distortion
  - HD3 increases by \((\frac{V_{DD1}}{V_{DD2}})^2\)
  - HD2 increases by \((\frac{V_{DD1}}{V_{DD2}})\)

Sampling Distortion

- SFDR \(\rightarrow\) sensitive to sampling distortion
  - improve linearity by:
    - Larger VDD
    - Higher sampling bandwidth
- Solutions:
  - Overdesign \(\rightarrow\) Larger switches
    - Increased switch charge injection
    - Increased nonlinear S&D junction cap.
  - Maximize VDD/VFS
    - Decreased dynamic range if VDD const.
  - Complementary switch
  - Constant & max. \(V_{GS} ? f(V_p)\)
Complementary Switch

- Complementary n & p switch advantages:
  - Increases the overall conductance
  - Linearize the switch conductance for the range $V_{tp} < V_{in} < V_{dd} - V_{tn}$

Complementary Switch Issues

Supply Voltage Evolution

- Supply voltage scales down with technology scaling
- Threshold voltages do not scale accordingly

Complementary Switch
Effect of Supply Voltage Scaling

- As supply voltage scales down input voltage range for constant $g_o$ shrinks
  - Complementary switch not effective when $V_{DD}$ becomes comparable to $V_i$

Boosted & Constant $V_{GS}$ Sampling

- Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
  - Switch overdrive voltage is independent of signal level
  - Error from finite $R_{ON}$ is linear (to first order)
  - Lower $R_{ON}$ achieved → lower time constant
**Constant $V_{GS}$ Sampling**

The diagram shows a boosted clock signal and an input signal. The input signal is labeled as the voltage at the switch source terminal.

**Constant $V_{GS}$ Sampling Circuit**

The circuit diagram includes components such as $V_{DD} = 3V$, $M1$ to $M11$, $C1$ to $C3$, and various switches and capacitors. The example specifies device sizes of 10µ/0.35µ and all capacitor sizes as 1pF.

This Example: All device sizes: 10µ/0.35µ
All capacitor size: 1pF
Clock Voltage Doubler

Clock period: 100ns

R1 & R2 = 1GOhm
\( \rightarrow \) dummy resistors added for simulation only

Constant \( V_{GS} \) Sampler: \( \Phi \) LOW

- Sampling switch M11 is OFF
- C3 charged to VDD
Constant $V_{GS}$ Sampler: $\Phi$ HIGH

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant $V_{GS} = VDD$

Constant $V_{GS}$ Sampling

Input Switch $V_{Gate}$
Chold Signal
Input Signal
Complete Circuit


Advanced Clock Boosting

Advanced Clock Boosting Technique

- Gate tracks average of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- SFDR = 76.5dB at \( f_{\text{in}} = 200\text{MHz} \) (measured)


Switch Off-Mode Feedthrough Cancellation

High-pass feedthrough paths past an open switch

Feedthrough cancellation with a dummy switch

Practical Sampling

\[ v_{\text{IN}} \xrightarrow{M_1} v_{\text{OUT}} \]

- \( R_{\text{SW}} = f(V_{\text{IN}}) \rightarrow \text{distortion} \)
- \( \text{Switch charge injection} \)

Sampling Switch Charge Injection

- First assume \( V_{\text{IN}} \) is a DC voltage
- When switch turns off \( \rightarrow \) offset voltage induced on \( C_s \)
- Why?
Sampling Switch Charge Injection

MOS xtor operating in triode region
Cross section view

• Channel \(\rightarrow\) distributed RC network
• Channel to substrate junction capacitance \(\rightarrow\) distributed & variable
• Over-lap capacitance \(C_{ov} = L_D \cdot W \cdot C_{ov}\) associated with GS & GD overlap

Switch Charge Injection
Slow Clock

• Since clock fall time >> device speed
  \(\Rightarrow\) During the period \((t- \to t_{off})\) current in channel discharges channel charge into low impedance signal source
• Only source of error \(\Rightarrow\) Charge transfer from \(C_{ov}\) into \(C_s\)
Switch Charge Injection
Slow Clock

\[
\Delta V = - \frac{C_{ov}}{C_{ov} + C_s} (V_i + V_{th} - V_L)
\]

where \( \epsilon = \frac{C_{ov}}{C_s} \); \( V_{ss} = \frac{C_{ov}}{C_s} (V_{th} - V_L) \)

Switch Charge Injection
Slow Clock- Example

\( C_{ov} = 0.3 \, fF / \mu \); \( C_s = 5 \, fF / \mu \); \( V_{th} = 0.5V \)

\( \epsilon = \frac{C_{ov}}{C_s} = \frac{12 \mu \times 0.3 \, fF / \mu}{1 \, pF} = -56\% \rightarrow 7\text{-bit} \)

\( V_{ss} = - \frac{C_{ov}}{C_s} (V_{th} - V_L) = -1.8 \, mV \)
Switch Charge Injection
Fast Clock

- Sudden gate voltage drop $\rightarrow$ no gate voltage to establish current in channel $\rightarrow$
  channel charge has no choice but to escape out towards S & D

\[
\Delta V_s = \frac{C_{ov}}{C_{ov} + C_s} (V_{th} - V_c) - \frac{1}{2} \frac{C_{ov} L}{C_s} \Delta V_t + V_{in} + V_{th}
\]

where $\Delta V_t = \frac{I}{2} W C_{ov} L$

\[
V_s = \frac{C_{ov}}{C_s} (V_{th} - V_c) - \frac{1}{2} \frac{W C_{ov} L (V_{th} - V_{in})}{C_s}
\]

- Assumption $\rightarrow$ channel charge divided equally between S & D
- Source of error $\rightarrow$ channel charge transfer + charge transfer from $C_{ov}$ into $C_s$
Switch Charge Injection
Fast Clock- Example

Both errors are a function of clock fall time, input voltage level, source impedance & sampling capacitance
Switch Charge Injection Error Reduction

- How do we reduce the error?
  → Reduce switch?

\[
\tau = R_{ox} C_i = \frac{C_i}{\mu_{Si} W L (V_{dd}-V_{ox})}
\]

\[
\Delta V = \frac{Q_{ox}}{2 C_i}
\]

\[
FOM = \tau \times \Delta V = \frac{C_i}{\mu_{Si} W L (V_{dd}-V_{ox})} \times \frac{W C_i L (V_H-V_L)}{2 C_i}
\]

\[
FOM = \frac{L^2}{\mu}
\]

→ Reducing switch size increases \(\tau\) → increased distortion → not a viable solution
→ Small \(\tau\) and \(\Delta V\) → use minimum channel length
→ For a given technology \(\tau \times \Delta V = \text{conts.}\)

Sampling Switch Charge Injection Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Charge sharing with \(C_{ov}\)
  - Channel charge transfer

- Issues:
  - DC offset
  - Input dependant error voltage → distortion

- Solutions:
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?
Switch Charge Injection
Complementary Switch

- In slow clock case if area of devices are equal → effect of overlap capacitor for n & p devices cancel to first order (matching n & p area)

\[ Q_{b,n} = W_n C_s I_n (V_H - V_L) \]
\[ Q_{b,p} = W_p C_s I_p (V_H - V_L - V_{th,n}) \]
\[ \Delta V_o = \frac{1}{2} \left( \frac{Q_{b,p}}{C_s} - \frac{Q_{b,n}}{C_s} \right) \]
\[ V_o = V_H (1 + \epsilon) + V_{in} \]
\[ \epsilon = \frac{1}{2} \frac{W_n C_s I_n + W_p C_s I_p}{C_s} \]

- In fast clock case
  - Offset cancelled for equal device area
  - Input voltage dependant error worse!
Switch Charge Injection
Dummy Switch

- Dummy switch same L as main switch but half W
- Main device clock goes low, dummy device goes high → dummy switch acquires same amount of channel charge main switch needs to lose
- Effective only if exactly half of the charge transferred to M2 and good matching between clock fall/rise

\[ W_{M2} = \frac{1}{2} W_{M1} \]

Switch Charge Injection
Dummy Switch

- To guarantee half of charge goes to each side → create the same environment on both sides
  - Add C equal to sampling capacitor to the other side of the switch + add fixed resistor
  - Degrades sampling bandwidth
**Dummy Switch Effectiveness Test**

- Dummy switch \( W = 1/2 W_{\text{main}} \)
- Note large \( L_s \) → good device area matching


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**Switch Charge Injection Bottom Plate Sampling**

- Switches \( M2A @ B \) are opened slightly earlier compared to \( M1A & B \) → Injected charge by the opening of \( M2AB \) is constant & eliminated when used differentially
- Since bottom plate of \( C_s \) is open when \( M1A & B \) are opened → no charge injected on \( C_s \)