EE247
Lecture 25

• Administrative
  – EE247 Final exam:
    – Date: Tues. Dec. 13th
    – Time: 12:30pm-3:30pm
    – Location: 285 Cory Hall

  • Closed book/course notes
  • No calculators/cell phones/PDAs/computers
  • Bring one 8x11 paper with your own notes
  • Final exam covers the entire course material unless specified

• Oversampled ADCs
  – 2nd order $\Sigma\Delta$ modulator
    • Practical implementation
      – Effect of various nonidealities on the $\Sigma\Delta$ performance
  • Higher order $\Sigma\Delta$ modulators
    – Cascaded modulators (multi-stage)
    – Single-loop single-quantizer modulators with multi-order filtering in the forward path
Oversampled ADCs

Last Lecture

Oversampled ADCs:
- Allows trading speed for resolution
- No stringent requirements imposed on analog building blocks
- Takes advantage of low cost, low power digital filtering
- Relaxed transition band requirements for analog anti-aliasing filters
- Further reduction of baseband quantization noise power by combining oversampling with clever use of feedback
  - By simply increasing oversampling ratio: 2X increase in sampling ratio \(\rightarrow\) 0.5-bit increase in resolution
  - Embedding the quantizer in a 1\(^{st}\) order feedback loop \(\rightarrow\) 1.5-bit increase is resolution per 2x increase in sampling rate
  - Adding a 2\(^{nd}\) loop \(\rightarrow\) 2.5-bit increase per 2x increase in sampling rate

ΣΔ Implementation

Practical Design Considerations

- Internal nodes scaling & clipping
- Finite opamp gain & linearity
- Capacitor ratio errors
- KT/C noise
- Opamp noise
- Power dissipation considerations
Switched-Capacitor Implementation 2\textsuperscript{nd} Order ΣΔ 
Nodes Scaled for Maximum Dynamic Range

• Modification (gain of \(\frac{1}{2}\) in front of integrators) reduce & optimize required signal range at the integrator outputs \(\sim 1.7x\) input full-scale (Δ)


2\textsuperscript{nd} Order ΣΔ Modulator 
Switched-Capacitor Implementation

• The \(\frac{1}{2}\) loss in front of each integrator implemented by choice of:

\[ C_2 = 2C_1 \]
2nd Order $\Sigma \Delta$

Effect of Integrator Maximum Signal Handling Capability on SNR

- Effect of 1st Integrator maximum signal handling capability on converter SNR


1st integrator maximum signal handling:
1.4, 1.5, 1.6, and 1.7X $\Delta$

2nd Order $\Sigma \Delta$

Effect of Integrator Maximum Signal Handling Capability on SNR

- Effect of 2nd Integrator maximum signal handling capability on SNR


2nd integrator maximum signal handling:
0.75, 1, 1.25, 1.5, and 1.75X $\Delta$
2nd Order ΣΔ
Effect of Integrator Finite DC Gain

\[ H(z)_{\text{ideal}} = \frac{C_s}{C_l} \times \frac{1}{1 - z^{-1}} \]
\[ H(z)_{\text{Finite DC Gain}} = \frac{C_s}{C_l} \times \frac{\frac{a}{1 + a + \frac{C_s}{C_l}}}{1 - \frac{1 + a}{1 + a + \frac{C_s}{C_l}} z^{-1}} \]

- Low integrator DC gain \(\Rightarrow\) Increase in total in-band noise
- Can be shown: If \(a > M\) (oversampling ratio) \(\Rightarrow\) Insignificant degradation in SNR
- Normally DC gain designed to be >> M in order to suppress nonlinearities
2\textsuperscript{nd} Order \(\Sigma\Delta\)

Effect of Integrator Finite DC Gain

- Example: \(a = 2M \rightarrow 0.4\text{dB}\) degradation in SNR


2\textsuperscript{nd} Order \(\Sigma\Delta\)

Effect of Comparator Non-Idealities on SD Performance

- 1-bit A/D \(\rightarrow\) Single comparator
  - Speed must be adequate for the operating sampling rate
  - Input referred offset- feedback loop suppresses the effect \(\rightarrow\) \(\Sigma\Delta\) performance not sensitive to input referred offset
  - Input referred noise- same as offset
  - Hysteresis= Minimum overdrive required to change the output
2nd Order ΣΔ
Comparator Hysteresis

Hysteresis = Minimum overdrive required to change the output

Æ Comparator hysteresis < Δ/40 does not affect SNR
Æ E.g. Δ=1V, comparator offset/hysteresis up to 25mV tolerable
2nd Order $\Sigma\Delta$

Effect Overall Integrator Gain Inaccuracy

- Gain of $\frac{1}{2}$ in front of integrators determined by ratio of $C_1/C_2$
- Effect of inaccuracy in ratio of $C_1/C_2$ inspected by simulation

2nd Order $\Sigma\Delta$

Effect of Integrator Overall Gain Inaccuracy

- Simulation show gain can vary by 20% w/o loss in performance
  - Confirms insensitivity of $\Sigma\Delta$ to component variations
- Note that for gain $>0.65$ system becomes unstable & SNR drops rapidly
2nd Order ΣΔ
Effect of Integrator Nonlinearities

With non-linearity added:

\[ v(kT + T) = u(kT) + \alpha_2 [u(kT)]^2 + \alpha_3 [u(kT)]^3 + \cdots \]
\[ + v(kT) + \beta_2 [v(kT)]^2 + \beta_3 [v(kT)]^3 + \cdots \]


- Simulation for single-ended topology
- Even order nonlinearities can be significantly attenuated by using differential circuit topologies

Effect of Integrator Nonlinearities

- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)


Effect of KT/C noise

- For the example of digital audio with 16-bit (100dB) & M=256
  - Cs=1pF → 6μVrms noise
  - If FS=2Vp-p then thermal noise @ -101dB → degrades overall SNR by < 3dB
  - Cs=1pF, CI=2pF → small capacitor area compared to Nyquist ADC
  - Since thermal noise provides some level of dithering → better not choose much larger capacitors!
2nd Order ΣΔ
Effect of Finite Opamp Bandwidth

Assumptions:
Opamp → does not slew
Opamp has only one pole → exponential settling

→ ΣΔ does not require high opamp bandwidth $f_u > 2f_s$ adequate
2nd Order ΣΔ
Effect of Slew Limited Settling

Assumption:
Opamp settling $\Rightarrow$ includes a single-pole setting of $\tau = 1/2f_s +$ slewing
$\Rightarrow$ Low slew rate degrades SNR rapidly increases quantization noise and causes signal distortion
$\Rightarrow$ Minimum slew rate of $1.2 \ (\Delta x f_s)$ required
Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces
- SPICE type simulators:
  - Normally used to test for gross circuit errors only
  - Too slow and inaccurate for performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities simultaneously as possible to verify whether there are interaction among non-idealities

Modulator Testing

- Should make provisions for testing the modulator (AFE) separate from the decimator (digital back-end)
- Data acquisition board used to collect 1-bit digital output at $f_s$ rate
- Analyze data in a PC environment or dedicated test equipment in manufacturing environments can be used
- Need to run DFT on the collected data and also make provisions to perform the function of digital decimation filter in software
- Typically, at this stage, parts of the design phase behavioral modeling effort can be utilized
- Good testing strategy vital for debugging/improving challenging designs

\[ \text{Filtered Sinwave} \rightarrow \text{AFE} \rightarrow \text{Data Acq.} \rightarrow \text{PC Matlab} \]
2nd Order $\Sigma\Delta$
Implementation Example: Digital Audio Application

- 5V supply, $\Delta = 4V_{p-p}$
- Minimum capacitor values computed based on -107dB noise wrt maximum signal
  - Max. inband $KT/C$ noise = $7\mu V_{rms}$
  - $C1 = (2kT)/(Mv_n^2) = 1pF$  $\quad C2 = 2C1$


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2nd Order $\Sigma\Delta$
Implementation Example: Digital Audio Applications

Measured Performance Summary
(Does Not Include Decimator)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range</td>
<td>98 dB (16 b)</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>94 dB</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>12.8 MHz</td>
</tr>
<tr>
<td>Oversampling Ratio</td>
<td>256</td>
</tr>
<tr>
<td>Output Rate</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Signal Band</td>
<td>23 kHz</td>
</tr>
<tr>
<td>Differential Input Range</td>
<td>4 V</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td>60 dB</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>13.8 mW</td>
</tr>
<tr>
<td>Area</td>
<td>0.139 mm$^2$</td>
</tr>
<tr>
<td>Technology</td>
<td>1-μm CMOS</td>
</tr>
</tbody>
</table>

2nd Order $\Sigma\Delta$

Implementation Example: Digital Audio Applications

2nd Order ΣΔ
Implementation Example: Digital Audio Applications

→ Measured & simulated spurious tones performance as a function of DC input signal
→ Sampling rate=12.8MHz, M=256

→ Measured & simulated noise tone performance for near zero DC input of 0.00088Δ
→ Sampling rate=12.8MHz, M=256
2nd Order $\Sigma\Delta$
Implementation Example: Digital Audio Applications

> Measured & simulated worst-case noise tone @ DC input of 0.00088\Delta
> Both indicate maximum tone @ 22.5kHz around -100dB level


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2nd Order $\Sigma\Delta$
Implementation Example: Integrator Opamp

- Class A/B opamp $\rightarrow$ High slew-rate
- S.C. common-mode feedback
- Input referred noise (both thermal and 1/f) important for high resolution performance
- Minimum required DC gain > M=256, usually DC gain designed to be much higher to suppress nonlinearities (particularly, for class A/B amps)
- Minimum required slew rate of $1.2(\Delta f_s) \rightarrow 65V/\mu s$
- Minimum opamp settling time constant $\rightarrow 1/2fs\sim30\text{ns}$

2nd Order $\Sigma\Delta$
Implementation Example: Comparator

- Comparator $\rightarrow$ simple design
- Minimum acceptable hysteresis or offset (based on analysis) $\rightarrow \Delta/40 \sim 100\text{mV}$


2nd Order $\Sigma\Delta$
Implementation Example: Subcircuit Performance

<table>
<thead>
<tr>
<th>Subcircuit Performance</th>
<th>Our computed minimum required</th>
<th>Over-Design Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>67 dB</td>
<td>x8</td>
</tr>
<tr>
<td>Unity-gain frequency</td>
<td>50 MHz</td>
<td>x2</td>
</tr>
<tr>
<td>Slew rate</td>
<td>350 V/µsec</td>
<td>x5</td>
</tr>
<tr>
<td>Linear output range</td>
<td>6 V</td>
<td>Output range $1.7\Delta=6.8V!$ x0.9</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>12.8 MHz</td>
<td></td>
</tr>
<tr>
<td>Integrator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling time constant</td>
<td>7.25 nsec</td>
<td>x4</td>
</tr>
<tr>
<td>Comparator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>13 mV</td>
<td>x7</td>
</tr>
</tbody>
</table>

Higher Order $\Sigma\Delta$ Modulators

- Extending $\Sigma\Delta$ Modulators to higher orders by adding integrators in the forward path (similar to 2nd order)
  - Issues with stability
- Two different architectural approaches used to implement $\Sigma\Delta$ modulators of order >2
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path
  - Cascade of lower order modulators (multi-stage)

Higher Order $\Sigma\Delta$ Modulators
Mult-Order Filter

\[
Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z)
\]

\[
NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}
\]

- Zeros of NTF (poles of $H(z)$) can be positioned to suppress baseband noise spectrum
- Main issue → Loop stability for 3rd and higher orders
Higher Order $\Sigma \Delta$ Modulators
Cascaded Modulators

- Cascade two or more stable $\Sigma \Delta$ stages
- Quantization error of each stage is quantized by the succeeding stage and subtracted digitally
- Order of noise shaping equals sum of the orders of the stages
- Quantization noise cancellation depends on the precision of analog signal paths
- Quantization noise further randomized $\rightarrow$ less limit cycle oscillation problems
- Typically, no potential instability

2-Stage Cascaded $\Sigma \Delta$ Modulators

- Main $\Sigma \Delta$ quantizes the signal
- The quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain
2nd Order (1-1) Cascaded \( \Sigma\Delta \) Modulators

\[
Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)
\]
\[
Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)
\]
\[
Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)
\]
\[
= z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z)
\]
\[
- (1 - z^{-1})^2E_2(z)
\]
\[
Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)
\]

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3rd Order Cascaded \( \Sigma\Delta \) Modulators

- Can implement 3rd order noise shaping with 1-1-1
- This is also called MASH (multi-stage noise shaping)
3rd Order (2-1) Cascaded ΣΔ Modulators

Advantages of 2-1 cascade:
- Low sensitivity to precision of analog paths
- Low spurious noise tones
- No potential instability

\[
Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2E_1(z)
\]
\[
Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})^2E_2(z)
\]
\[
Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2Y_2(z)
\]

3rd order noise shaping

\[
Y(z) = z^{-3}X(z) - (1 - z^{-1})^3E_2(z)
\]

Sensitivity of (1-1-1) Cascaded ΣΔ Modulators to Matching of Analog & Digital Gains

Accuracy of < 0.1%

\(\Rightarrow 2\text{dB loss in DR}\)
Sensitivity of (2-1) Cascaded $\Sigma\Delta$ Modulators to Matching Error

![Graph showing sensitivity of (2-1) cascaded $\Sigma\Delta$ modulators to matching error.]

Main advantage of 2-1 cascade compared to 1-1-1 topology:
- Low sensitivity to precision of analog paths (over one order of magnitude!)


2-1 Cascaded $\Sigma\Delta$ Modulators

![Diagram of 2-1 cascaded $\Sigma\Delta$ modulators.]

2-1 Cascaded $\Sigma\Delta$ Modulators

Effect of gain parameters on signal-to-noise ratio

Comparison of 2nd order & Cascaded (2-1) $\Sigma\Delta$ Modulator

Digital Audio Application, $f_N=50kHz$

<table>
<thead>
<tr>
<th></th>
<th>Brandt, JSSC 4/91</th>
<th>Williams, JSSC 3/94</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
<td>2nd order</td>
<td>(2+1) Order</td>
</tr>
<tr>
<td>Architecture</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>98dB (16-bits)</td>
<td>104dB (17-bits)</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>94dB</td>
<td>98dB</td>
</tr>
<tr>
<td>Oversampling rate</td>
<td>256 (theoretical $\rightarrow$ SNR=109dB)</td>
<td>128 (theoretical $\rightarrow$ SNR=128dB)</td>
</tr>
<tr>
<td>Differential input range</td>
<td>4Vppd 5V supply</td>
<td>8Vppd 5V supply</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>13.8mW</td>
<td>47.2mW</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.39mm$^2$</td>
<td>5.2mm$^2$</td>
</tr>
</tbody>
</table>
2-1 Cascaded $\Sigma\Delta$ Modulators
Measured Dynamic Range Versus Oversampling Ratio


Summary

• Oversampled ADCs decouple SQNR from circuit complexity and accuracy

• If a 1-Bit DAC is used, the converter is inherently linear—indeedependent of component matching

• Typically, used for high resolution & low frequency applications — e.g. digital audio

• 2nd order $\Sigma\Delta$ used extensively due to lower levels of limit cycle related spurious tones

• $\Sigma\Delta$ modulators of order greater than 2:
  – Single-loop, single-quantizer modulators with multi-order filtering in the forward path
  – Cascaded (multi-stage) modulators
Bandpass $\Delta\Sigma$ Modulator

- Replace the integrator in 1st order lowpass $\Sigma\Delta$ with a resonator
  \[ \rightarrow 1^{\text{st}} \text{order bandpass } \Sigma\Delta \]

**Key Point:**

- NTF $\rightarrow$ notch type shape
- STF $\rightarrow$ bandpass shape

Ref:
Paolo Cusinato, et. al, “A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range”, IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
Bandpass $\Sigma\Delta$ Modulator Dynamic Range
As a Function of Modulator Order ($K$)

- Bandpass $\Sigma\Delta$ resolution for order $K$ is the same as lowpass $\Sigma\Delta$ resolution with order $L = K/2$

Example: Sixth-Order Bandpass $\Sigma\Delta$ Modulator

Ref:
Paolo Cusinato, et. al, “A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range”, IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
**Bandpass $\Sigma\Delta$ Characteristics**

- Oversampling ratio defined as $f_s/2B$ where $B =$ bandpass filter bandwidth
- Typically, sampling frequency is chosen to be $4f_{center}$ where $f_{center} =$ bandpass filter center frequency
- STF has a bandpass shape while NTF has a notch shape
- To achieve same resolution as lowpass, needs twice as many integrators