EE247 Lecture 26

• Administrative
  – Final exam:
    • Date: Tues. Dec. 13th
    • Time: 12:30pm-3:30pm
    • Location: 285 Cory
    • Office hours this week: Tues: 2:30p to 3:30p
      Wed: 1:30p to 2:30p (extra)
      Thurs: 2:30p to 3:30p
  • Closed book/course notes
  • No calculators/cell phones/PDAs/Computers
  • You can bring two 8x11 paper with your own notes
  • Final exam covers the entire course material

EE247 Lecture 26

• Higher order $\Sigma \Delta$ modulators
  – Last lecture $\rightarrow$ Cascaded $\Sigma \Delta$ modulators (MASH)
  – This lecture $\rightarrow$ Bandpass $\Sigma \Delta$ modulators
  – This lecture $\rightarrow$ Forward path multi-order filter
    • Example: 5th order Lowpass $\Sigma \Delta$
      – Modeling
      – Noise shaping
      – Effect of various nonidealities on the $\Sigma \Delta$ performance
Bandpass $\Delta \Sigma$ Modulator

- Replace the integrator in 1st order lowpass $\Sigma \Delta$ with a resonator
  $\rightarrow$ 2nd order bandpass $\Sigma \Delta$

Key Point:

Ref:
Paolo Cusinato, et. al, “A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range”, IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
Bandpass $\Sigma\Delta$ Characteristics

- Oversampling ratio defined as $f_s/2B$ where $B =$ bandpass filter bandwidth
- Typically, sampling frequency is chosen to be $f_s = 4f_{\text{center}}$ where $f_{\text{center}} =$ bandpass filter center frequency
- STF has a bandpass shape while NTF has a notch shape
- To achieve same resolution as lowpass, need twice as many integrators

Bandpass $\Sigma\Delta$ Modulator Dynamic Range
As a Function of Modulator Order (K)

- Bandpass $\Sigma\Delta$ resolution for order K is the same as lowpass $\Sigma\Delta$ resolution with order $L = K/2$
Example: Sixth-Order Bandpass ΣΔ Modulator

Simulated noise transfer function

Simulated signal transfer function

Ref:
Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

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Example: Sixth-Order Bandpass ΣΔ Modulator

**Features & Measured Performance**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog input full-scale</td>
<td>4.4V (differential)</td>
</tr>
<tr>
<td>Sampling frequency (f_s)</td>
<td>42.8MHz</td>
</tr>
<tr>
<td>Center frequency (f_0)</td>
<td>10.7MHz</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>200kHz</td>
</tr>
<tr>
<td>OSR</td>
<td>107</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>74dB (200kHz band)</td>
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<tr>
<td></td>
<td>88dB (9kHz band)</td>
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<tr>
<td>Peak SNDR</td>
<td>61dB</td>
</tr>
<tr>
<td>IMD (0-15dB)</td>
<td>71dBc</td>
</tr>
<tr>
<td>Active die area</td>
<td>1mm²</td>
</tr>
<tr>
<td>Power supply</td>
<td>3.3V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>76mW (adaptive biasing)</td>
</tr>
<tr>
<td></td>
<td>126mW (standard biasing)</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35μm CMOS</td>
</tr>
</tbody>
</table>

Ref:
Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001
Higher Order Lowpass $\Sigma \Delta$ Modulators

Forward Path Multi-Order Filter

\[ Y(z) = \frac{H(z)}{1 + H(z)} Y(z) + \frac{1}{1 + H(z)} E(z) \]

$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}$

- Zeros of NTF (poles of $H(z)$) can be positioned to flatten baseband noise spectrum
- Main issue → Ensuring stability for 3rd and higher orders

Overview

- Building behavioral models in stages

- A 5\textsuperscript{th}-order, 1-Bit $\Sigma \Delta$ modulator
  - Noise shaping
  - Complex loop filters
  - Stability
  - Voltage scaling
  - Effect of component non-idealities
Building Models in Stages

- When modeling a complex system like a 5th-order $\Sigma\Delta$ modulator, model development proceeds in stages
  - Each stage builds on its predecessor

- Design goal → detect and eliminate problems at the highest possible level of abstraction
  - Each successive stage consumes progressively more engineering time

- Our $\Sigma\Delta$ model development proceeds in stages:
  - Stage 0 gets to the starting line: Collect references, talk to veterans
  - Stage 1 develops a practical system built with ideal sub-circuits & simulated
  - Stage 2 models key sub-circuit non-idealities and translates the results into real-world sub-circuit performance specifications
  - Real-world model development includes a critical stage 3: Adding elements to earlier stages to model significant surprises found in silicon

Stage 1

- In stage 1, we’ll study a model for a practical $\Sigma\Delta$ modulator topology built with ideal blocks

- Stage 1 model focus
  - Signal amplitudes
  - Stability
    - Identifying worst-case inputs
    - Unstable systems can’t graduate to stage 2
  - Quantization noise shaping

- Verify performance and functionality for all regions of operation, find and test worst-case inputs
- Determine appropriate performance metrics and build the software infrastructure
ΣΔ Modulator Design

• Procedure
  – Establish requirements
  – Design noise-transfer function, NTF
  – Determine loop-filter, H
  – Synthesize filter
  – Evaluate performance,
  – Establish stability criteria


Example: Modulator Specification

• Example: Audio ADC
  – Dynamic range DR 18 Bits
  – Signal bandwidth B 20 kHz
  – Nyquist frequency \( f_N \) 44.1 kHz
  – Modulator order L 5
  – Oversampling ratio \( M = \frac{f_s}{f_N} \) 64
  – Sampling frequency \( f_s \) 2.822 MHz

• The order L and oversampling ratio M are chosen based on
  – SQNR > 120dB
Modulator Block Diagram

\[
\begin{align*}
\text{STF} & = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \\
\text{NTF} & = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}
\end{align*}
\]

Approach:
Design NTF and solve for \( H(z) \)

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Noise Transfer Function, NTF(z)

```matlab
% stop-band attenuation Rstop ...
Rstop = 80;
[b,a] = cheby2(L, Rstop, 1/M, 'high');

% normalize
b = b/b(1);
NTF = filt(b, a, 1/fs);
```

---

[Graph of NTF vs. Frequency]
Loop-Filter, $H(z)$

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}$$

$$\rightarrow H(z) = \frac{1}{\text{NTF}} - 1$$

**Modulator Topology**

**Simulation Model**
Rounded Filter Coefficients

\[
\begin{align*}
  a_1 &= 1; & k_1 &= 1; & b_1 &= 1/1024; \\
  a_2 &= 1/2; & k_2 &= 1; & b_2 &= 1/16-1/64; \\
  a_3 &= 1/4; & k_3 &= 1/2; \\
  a_4 &= 1/8; & k_4 &= 1/4; \\
  a_5 &= 1/8; & k_5 &= 1/8; & g &= 1; \\
\end{align*}
\]

Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1

5th Order Noise Shaping

- Mostly quantization noise, except at low frequencies
- Let’s zoom into the baseband portion…

![Graph showing output spectrum and integrated noise](image-url)
5th Order Noise Shaping

**Output Spectrum [dBWN] / Int. Noise [dBFS]**

- **Quantization noise** -130dBFS at band edge!
- **Digital decimation filter** removes out-of-band quantization noise

- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise
In-Band Noise Shaping

- Lot's of gain in the pass-band
- Remember that
  - \( \text{NTF} \approx 1/H \)
  - \( \text{STF} = H/(1+H) \)

Output Spectrum

- \(|H(z)| \) maxima align up with noise minima

Stability Analysis

- Approach: linearize quantizer and use linear system theory!
- Effective quantizer gain
  \[
  G_{\text{eff}}^2 = \frac{y^2}{q^2}
  \]
- Obtain \( G_{\text{eff}} \) from simulation
Modulator Root-Locus

As $G_{\text{eff}}$ increases, poles of STF move from:
- poles of $H(z)$ ($G_{\text{eff}} = 0$)
- zeros of $H(z)$ ($G_{\text{eff}} = \infty$)

Pole-locations inside unit-circle correspond to stable STF and NTF:
- $G_{\text{eff}} > 0.45$ for stability

Effective Quantizer Gain, $G_{\text{eff}}$

- Large inputs $\Rightarrow$ comparator input grows
- Output is fixed ($\pm 1$)
  - $G_{\text{eff}}$ drops
  - modulator unstable for large inputs

Solution:
- Limit input amplitude
- Detect instability (long sequence of $+1$ or $-1$) and reset integrators
- Beware of "worst-case inputs" (e.g. square waves near high-Q poles – attenuate with anti-aliasing filter)
- Note that signals grow slowly for nearly stable systems $\Rightarrow$ use long simulations
Internal Node Voltages

- Internal signal amplitudes are weak function of input level (except near overload)
- Maximum peak-to-peak voltage swing approach ±10V! Exceed supply voltage!
- Solutions:
  - Reduce $V_{ref}$ ??
  - Node scaling

Internal Node Voltage Scaling

- If we scale filter $k_1$ by 0.1,
  - All state variables and Q scale by 0.1
  - But since the comparator output is fixed and input is decreased by 10, G increases 10X

- The change in $k_1$ doesn’t change the shape of the root locus, either
  - The effective gain for each root position is increased 10X
  - $G_{new} = 10G_{old} \Rightarrow G_{new} > 4.5$ is thus required to ensure stability
5th Order Modulator – Scaling

Only the sign of Q matters, so we can make $k_1$ whatever we want without changing the 1-Bit data at all.

Loop Voltage Scaling (cont.)

- Note that $\dot{3}$, $\dot{4}$, and $\dot{5}$ have substantially larger swings than $\dot{1}$ and $\dot{2}$

- Just about any filter topology allows node scaling which change internal state variable amplitudes without changing the filter output (recall filter node scaling)
  - The next slide shows an example
Node Scaling Example:
3rd Integrator Output Voltage Scaled by $\alpha$

$$V_{\text{new}} = V_{\text{old}} \cdot \alpha$$

Voltage Scaling

- Integrator output range is fine now
- But: maximum input signal limited to -5dB (-7dB with safety) – fix?
Input Range Scaling

Increasing the DAC levels by \( g \) reduces the analog to digital conversion gain:

\[
\frac{D_{out}(z)}{V_{in}(z)} = \frac{H(z)}{1 + gH(z)} \cong \frac{1}{g}
\]

Scaling the DAC output levels adjusts the modulator input range

- If \( V_{in} \) and the DAC outputs are scaled up by the same factor \( g \), the 1-Bit data is completely unchanged.

- Note that increasing the range also increases the quantization noise→ the dynamic range and peak SQNR remain constant!

- If the DAC output levels are increased and the analog full scale is held constant, the stability margin improves… at the expense of reduced SQNR.
Scaled Stage 1 Model

\[ g = 2.5; \]

2dB safety margin for stability

Effective Quantizer Gain

stable

unstable

Input [dBV]

Loop filter peak voltages [V]

Input [dBV]
5th Order Modulator
Final Parameters

Summary

- Stage 1 model verified – stable and meets SQNR specification

- Stage 2 issues in 5th order ΣΔ modulator
  - DC inputs
  - Spurious tones
  - Dither
  - kT/C noise
**5th Order Noise Shaping**

- Input: 0.1V, sinusoid
- 216 point DFT
- 30 averages
- Note: Large spurious tones in the vicinity of fs/2
- Let us check whether tones appear in-band?

**In-Band Noise**

- In-Band quantization noise: -120dB!
- Note: No in-band tones!
- While Large spurious tones appear in the vicinity of fs/2
**5th Order Noise Shaping**

- Input: 0.1V, sinusoid
- 2^{15} point DFT
- 30 averages

**Out-of-Band vs In-Band Signals**

- A digital (low-pass) filter with suitable coefficient precision can eliminate out-of-band quantization noise
- No filter can attenuate unwanted in-band components without attenuating the signal
- We’ll spend some time making sure the components at \(f_s/2-Nf_{in}\) will not “mix” down to the signal band
- But first, let’s look at the modulator response to small DC inputs (or offset) …
**ΣΔ Tones Generated by Small DC Input Signals**

Simulation technique:
A random 1st sample randomizes the noise from DC input and enables averaging. Otherwise the small tones will not become visible.

**Limit Cycles**

- Representing a DC term with a −1/+1 pattern … e.g.

\[
\frac{1}{11} \rightarrow \begin{pmatrix}
\frac{-1}{1}, & \frac{1}{2}, & \frac{-1}{3}, & \frac{1}{4}, & \frac{-1}{5}, & \frac{1}{6}, & \frac{-1}{7}, & \frac{1}{8}, & \frac{-1}{9}, & \frac{1}{10}, & \frac{1}{11}
\end{pmatrix}
\]

- Spectrum:

\[
\frac{L}{11}, \frac{2L}{11}, \frac{3L}{11}, \ldots
\]
Limit Cycles

- The frequency of the tones are indeed quite predictable
  - Fundamental
    \[ f_\delta = f_s \frac{V_{DC}}{V_{DAC}} \]
    \[ = 3 \text{MHz} \frac{5 \text{mV}}{2.5 \text{V}} \]
    \[ = 6 \text{kHz} \]
  - Tone velocity (useful for debugging)
    \[ \frac{df_\delta}{dV_{DC}} = \frac{f_s}{V_{DAC}} \]
    \[ = \frac{df_\delta}{dV_{DC}} = 1.2 \text{kHz/mV} \]
  - Note: For digital audio in this case DC signal > 20mV generates tone
    with \( f_\delta > 24 \text{kHz} \) → out-of-band → no problem

ΣΔ Spurious Tones

Effect of Small DC Input @ Vicinity of \( f_s/2 \)
ΣΔ Spurious Tones

- In-band spurious tones look like signals
- Can be a major problem in some applications
  - E.g. audio → even tones with power below the quantization noise floor can be audible
- Spurious tones near \( f_s/2 \) can be aliased down into the signal band
  - Since they are often strong, even a small amount of aliasing can create a major problem
  - We will look at mechanisms that alias tones later
- First let’s look at dither as a means to reduce or eliminate in-band spurious tones

Dither

- DC inputs can be represented by many possible bit patterns
- Including some that are random (non-periodic) but still average to the desired DC input
- The spectrum of such a sequence has no spurious tones
- How can we get a ΣΔ modulator to produce such “randomized” sequences?
Dither

• The target DR for our audio $\Sigma \Delta$ is 18 Bits, or 113dB
• Designed SQNR~120dB allows thermal noise to dominate at -115dB level
• Let’s choose the sampling capacitor such that it limits the dynamic range:

$$DR = \frac{\frac{1}{2}(V_{FS})^2}{V_n^2} \quad V_{FS} = Wp$$

$$\rightarrow \quad \sqrt{V_n} = \frac{1}{\sqrt{2DR}} (V_{FS}) = 1 \mu V$$

Effect of Dither on In-Band Spurious Tones

- Thermal noise added at the input of the 1st integrator
- In-band spurious tones disappear
- Note: they are not just buried
- How can we tell?
Effect of Dither on Spurious Tones Near $f_s/2$

Key point: Dither at an amplitude which eliminate the in-band tones has virtually no effect on tones near $f_s/2$.

kT/C Noise

- So far we’ve looked at noise added to the input of the $\Sigma\Delta$ modulator, which is also the input of the first integrator.

- Now let’s add noise also to the input of the second integrator.

- Let’s assume a 1/16 sampling capacitor value for the 2$^{nd}$ integrator wrt the 1$^{st}$ integrator.
  - This gives 4$\mu$V rms noise.
**kT/C Noise**

- 5mV DC input
- Noise from 2nd integrator smaller than 1st integrator noise shaped
- Why?

**Output Spectrum [dBWN] / Int. Noise [dBV]**

*No noise*
*1st Integrator*
*2nd Integrator*

**Effect of Integrator kT/C Noise**

- Noise from 1st integrator is referred directly to the input
- Noise from 2nd integrator is first-order noise shaped
- Noise from subsequent integrators → attenuated even further
  → Especially for high oversampling ratios, only the first 1 or 2 integrators add significant thermal noise. This is true also for other imperfections.
Dither

- No practical amount of dither eliminates the tones near $f_s/2$

Full-Scale Inputs

- With practical levels of thermal noise added, let’s try a 5kHz sinusoidal input near full-scale
  - No distortion is visible in the spectrum
    - 1-Bit modulators are intrinsically linear
    - But tones exist at high frequencies
      → To the oversampled modulator, a sinusoidal input looks like two “slowly” alternating DCs … hence giving rise to limit cycles
Recap

- Dither successfully removes in-band tones that would corrupt the signal
- The high-frequency tones in the quantization noise spectrum will be removed by the digital filter following the modulator
- What if some of these strong tones are demodulated to the base-band prior to digital filtering?
- Why would this happen?
  → Vref Interference
**V_{\text{ref}} Interference via Modulation**

\[
x_1(t) = X_1 \cos(\omega_1 t) \\
x_2(t) = X_2 \cos(\omega_2 t) \\
x_1(t) \times x_2(t) = \frac{X_1 X_2}{2} [\cos(\omega_1 t + \omega_2 t) + \cos(\omega_1 t - \omega_2 t)]
\]

---

**Modulation via DAC**

\[
y(t) = D_{\text{out}} = \pm 1 \\
V_{\text{ref}} = 2.5V + \text{Im}V f_s/2 \text{ square wave} \\
v(t) = v(t) \times V_{\text{ref}}
\]
Modulation via DAC

D\text{\textsubscript{OUT}} spectrum

V\text{\textsubscript{ref}} spectrum

interferer

convolution yields sum of red and green, mirrored tones and noise appear in band

0 \quad f_s/2 \quad f_s

\textbf{V_{\text{ref}} Interference via Modulation}

Output Spectrum [dBWN]

Key Point:
In high resolution ΣΔ modulators, V\text{\textsubscript{ref}} interference via modulation can significantly limit the maximum dynamic range

Frequency [kHz]

0 dB (1 dB/dB)
Symmetry of the spectra at $f_s/2$ and DC confirm that this is modulation.

$V_{\text{ref}}$ Spurious Tone Velocity vs Native Tone Velocity

- Native tone velocity $\Rightarrow 1.2\text{kHz/mV}$
- Aliased tone velocity $\Rightarrow 0.6\text{kHz/mV}$

$V_{\text{ref}}$ Interference via Modulation
Simulations performed to verify the effect of the DAC reference contamination via output signal interference particularly in the vicinity of $f_s/2$

- Interference modulates the high-frequency tones
- Since the high frequency tones are strong, a small amount ($1\mu V$) of interference suffices to create audible base-band tones
- Stronger interference ($1mV$) not only aliases spurious tones but elevated raises noise floor by aliasing high frequency quantization noise
- Amplitude of modulated tones is proportional to interference
- The velocity of modulated tones is half that of the native tones
- Such differences help debugging of silicon
- How clean does the reference have to be?
Summary

• Our stage 2 model can drive almost all capacitor sizing decisions
  – Gain scaling
  – kT/C noise
  – Dither

• Dither quite effective in the elimination of native in-band tones

• Extremely clean & well-isolated \( V_{\text{ref}} \) is required for high-dynamic range applications e.g. digital audio

• Next we will add relevant component imperfections:
  \( \rightarrow \) Effect of component nonlinearities on \( \Sigma\Delta \) performance