EE247
Lecture 17

- **DAC Converters** (continued)
  - Dynamic element matching
    - DAC reconstruction filter
- **ADC Converters**
  - Sampling
    - Thermal noise due to switch resistance
    - Sampling switch bandwidth limitations
    - Switch induced distortion
      - Sampling switch conductance dependence on input voltage
      - Clock voltage boosters
    - Sampling switch charge injection & clock feedthrough

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**Summary of Last Lecture**

- **DAC Converters** (continued)
  - Segmented current-switched DACs
  - DAC dynamic non-idealities
  - DAC design considerations
  - Self calibration techniques
  - Current copiers
A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

16bit DAC (6+10)- MSB DAC uses calibrated current sources

clock

data input

data register

clock

coarse decoder

65-stage shift register

2-way current switches

2-way current switches

10-bit binary current divider

64 calibrated current sources

spare current

calibration switching network

calibration circuitry

V_{out}

Current Divider 

1/2

1/2
Current Divider Inaccuracy due to Device Mismatch

M1 & M2 mismatch results in the two output currents not being exactly equal:

\[ I_d = \frac{I_{d1} + I_{d2}}{2} \]

\[ \frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d} \]

\[ \frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{TH}} \left( \frac{dW}{W_L} + dV_{TH} \right) \]

Problem: Device mismatch could severely limit DAC accuracy

Use of dynamic element matching (next few pages)

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IEEE JOURNAL OF SOLID-STATE CIRCuits, VOL. SC-11, NO. 6, DECEMBER 1976

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASCHHE

Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.
Dynamic Element Matching

During $\Phi_1$

\[
I_1^{(1)} = \frac{1}{2} I_0 (1 + \Delta_I)
\]

\[
I_1^{(2)} = \frac{1}{2} I_0 (1 - \Delta_I)
\]

During $\Phi_2$

\[
I_2^{(1)} = \frac{1}{2} I_0 (1 + \Delta_I)
\]

\[
I_2^{(2)} = \frac{1}{2} I_0 (1 - \Delta_I)
\]

Average of $I_2$:

\[
\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2}
\]

\[
= \frac{I_0 (1 - \Delta_I) + (1 + \Delta_I)}{2}
\]

\[
= \frac{I_0}{2}
\]

Note:
For optimum current division accuracy → clock frequency is divided by two for each finer division

Problem: Frequency of operation drastically reduced

Note: What if the same clock frequency is used?

Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Error analysis results.

Note: If the same clock frequency is used?
Dynamic Element Matching

During $\Phi_1$

\[
\begin{align*}
I_{11}^1 &= \frac{1}{4} I_o (1 + \Delta_1) \\
I_{12}^1 &= \frac{1}{4} I_o (1 - \Delta_1) \\
I_{11}^2 &= \frac{1}{4} I_o (1 + \Delta_2) \\
I_{12}^2 &= \frac{1}{4} I_o (1 - \Delta_2)
\end{align*}
\]

\[
\langle I_1 \rangle = \frac{I_{11}^1 + I_{12}^1}{2} = \frac{I_o}{4} (1 + \Delta_1) \\
\langle I_2 \rangle = \frac{I_{11}^2 + I_{12}^2}{2} = \frac{I_o}{4} (1 + \Delta_2)
\]

E.g. $\Delta_1 = \Delta_2 = 1\% \rightarrow$ matching error is $(1\%)^2 = 0.01\%$

During $\Phi_2$

\[
\begin{align*}
I_{21}^1 &= \frac{1}{4} I_o (1 + \Delta_1) \\
I_{22}^1 &= \frac{1}{4} I_o (1 - \Delta_1) \\
I_{21}^2 &= \frac{1}{4} I_o (1 + \Delta_2) \\
I_{22}^2 &= \frac{1}{4} I_o (1 - \Delta_2)
\end{align*}
\]

\[
\langle I_2 \rangle = \frac{I_{21}^1 + I_{22}^1}{2} = \frac{I_o}{4} (1 + \Delta_1) \\
\langle I_3 \rangle = \frac{I_{21}^2 + I_{22}^2}{2} = \frac{I_o}{4} (1 + \Delta_2)
\]

During $\Phi_1$

\[
\begin{align*}
I_{11}^3 &= \frac{1}{4} I_o (1 + \Delta_1) \\
I_{12}^3 &= \frac{1}{4} I_o (1 - \Delta_1) \\
I_{11}^4 &= \frac{1}{4} I_o (1 + \Delta_2) \\
I_{12}^4 &= \frac{1}{4} I_o (1 - \Delta_2)
\end{align*}
\]

\[
\langle I_4 \rangle = \frac{I_{11}^3 + I_{12}^3}{2} = \frac{I_o}{4} (1 + \Delta_1) \\
\langle I_5 \rangle = \frac{I_{11}^4 + I_{12}^4}{2} = \frac{I_o}{4} (1 + \Delta_2)
\]

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASCHTE

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL <0.25LSB!

12-Bit D/A Test Chip

<table>
<thead>
<tr>
<th>D/A NETWORK DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution : 12 bit</td>
</tr>
<tr>
<td>Accuracy : 1.5, 1.3, or 0.75 (linear)</td>
</tr>
<tr>
<td>Output current : 2mA</td>
</tr>
<tr>
<td>Temp. coeff. of output current : ±50 ppm/°C</td>
</tr>
<tr>
<td>Voltage coeff of output current : ±1ppm/V</td>
</tr>
<tr>
<td>Chip size : 2.5 x 2.5 mm</td>
</tr>
<tr>
<td>Max. clock freq. for dynamic matching : 100 kHz</td>
</tr>
<tr>
<td>Power supply : ±5V</td>
</tr>
</tbody>
</table>
20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Bernd Schafferer and Richard Adams

Example: State-of-the-Art current steering DAC

Segmented:
- 6bit unit-element
- 8bit binary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>14 Bit</th>
<th>1.4 GSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14</td>
<td>GSPS</td>
</tr>
<tr>
<td>DNL</td>
<td>+/- 0.8</td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>+/- 2.1</td>
<td>LSB</td>
</tr>
<tr>
<td>SFDR @ 1.0 GSPS</td>
<td>&gt; 60</td>
<td>dB</td>
</tr>
<tr>
<td>IMD @ 1.0 GSPS</td>
<td>&gt; 64</td>
<td>dBC</td>
</tr>
<tr>
<td>NSD @ f_{out} = 400MHz</td>
<td>-155</td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>Power (Core) @ 1.4GSPS</td>
<td>200</td>
<td>mW</td>
</tr>
<tr>
<td>Power (Total) @ 1.4GSPS</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>Area (Core)</td>
<td>0.8</td>
<td>mm²</td>
</tr>
<tr>
<td>Area (Chip)</td>
<td>6.25</td>
<td>mm²</td>
</tr>
</tbody>
</table>

Layout Tree Structures

- CLK
- OUTPUT CURRENTS
- DATA
- VCAS
- DECODER
- SWITCHES
- CASCODES
- SEGMENT CURRENT
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output \(\rightarrow\) staircase form
- Some applications require filtering (smoothing) of DAC output
  \(\rightarrow\) reconstruction filter

DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for \(\sin x/x\) droop
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter

- Digital and SC filter possible only in combination with oversampling (signal bandwidth $B < f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band $\sin(x)/x$ amplitude droop associated with the inherent DAC S/H function

Reconstruction Filters

DAC Reconstruction Filter

Example: Voice-Band CODEC Receive Path

Note: $f_{sig}^{max} = 3.4kHz$
$f_{DAC} = 8kHz$

$\Rightarrow \sin(\pi f_{sig}^{max} \times T_s)/(\pi f_{sig}^{max} \times T_s) = -2.75$ dB droop due to DAC $\sin(x)/x$ shape

Summary
D/A Converter

- D/A architecture
  - Unit element – complexity proportional to $2^B$ - excellent DNL
  - Binary weighted - complexity proportional to $B$ - poor DNL
  - Segmented- unit element $MSB(B_1)$+ binary weighted $LSB(B_2)$
    $\rightarrow$ complexity proportional $((2^{B_1}-1) + B_2)$ - DNL compromise between the two

- Static performance
  - Component matching

- Dynamic performance
  - Time constants, Glitches

- DAC improvement techniques
  - Symmetrical switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching

- Depending on the application, reconstruction filter may be needed

What Next?

- ADC Converters:
  - Need to build circuits that "sample"
  - Need to build circuits for amplitude quantization
Analog-to-Digital Converters

- Two categories:
  - Nyquist rate ADCs \( f_{\text{sig}}^{\text{max}} \sim 0.5f_{\text{sampling}} \)
    - Maximum achievable signal bandwidth higher compared to oversampled type
    - Resolution limited to max. 12-14 bits
  - Oversampled ADCs \( f_{\text{sig}}^{\text{max}} \ll 0.5f_{\text{sampling}} \)
    - Maximum possible signal bandwidth lower compared to nyquist
    - Maximum achievable resolution high (18 to 20 bits!)

MOS Sampling Circuits
Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{IN}$ onto the capacitor $C$

  → Output Dirac-like pulses with amplitude equal to $v_{IN}$ at the time of sampling

- In practice not realizable!

Ideal Track & Hold Sampling

- $V_{out}$ tracks input for ½ clock cycle when switch is closed
- Acquires exact value of $V_{in}$ at the instant the switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)
Ideal T/H Sampling

- Continuous Time
- T/H signal (Sampled-Data Signal)
- Clock
- Discrete-Time Signal

Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Finite $R_{sw} \rightarrow$ limited bandwidth $\rightarrow$ finite acquisition time
- $R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection & clock feedthrough
- Clock jitter
**kT/C Noise**

- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in \( \text{Total noise variance} = \frac{kT}{C} \) at the output (see noise analysis in Lecture 1)
- In high resolution ADCs kT/C noise at times dominates overall minimum signal handling capability (power dissipation considerations).

**Sampling Network kT/C Noise**

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise:

Assumption: \( \Rightarrow \) Nyquist rate ADC

For a Nyquist rate ADC: Total quantization noise power \( = \frac{\Delta^2}{12} \)

Choose \( C \) such that thermal noise level is less (or equal) than Q noise

\[
\frac{k_BT}{C} \leq \frac{\Delta^2}{12}
\]

\[
\Rightarrow \quad C \geq 12k_BT \left( \frac{2^B-1}{V_{FS}} \right)^2
\]

\[
\Rightarrow \quad C \geq 12k_BT \times \frac{2^{2B}}{V_{FS}^2}
\]
Sampling Network $kT/C$ Noise

$$C \geq 12kT \frac{2^B}{V_{FS}}$$

<table>
<thead>
<tr>
<th>$B$</th>
<th>$C_{\min}$ ($V_{FS} = 1V$)</th>
<th>$C_{\min}$ ($V_{FS} = 0.5V$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
<td>0.012 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
<td>2.4 pF</td>
</tr>
<tr>
<td>14</td>
<td>13 pF</td>
<td>52 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
<td>824 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
<td>211,200 pF</td>
</tr>
</tbody>
</table>

The large area required for $C$ limits the highest achievable resolution for Nyquist rate ADCs. Oversampling results in a reduction of the required value for $C$ (will be covered in oversampled converter lectures).

Sampling Acquisition Bandwidth

- The resistance $R$ of switch $S1$ turns the sampling network into a lowpass filter with finite time constant:
  $$\tau = RC$$

- Assuming $V_{in}$ is constant during the sampling period and $C$ is initially discharged

- Need to allow enough time for the output to settle to less than 1 ADC LSB determines the minimum duration for $\phi_1$ or maximum clock frequency
Sampling: Effect of Switch On-Resistance

\[ V_{in} - V_{out} \ll \Delta \quad \text{since} \quad V_{out} = V_{in} (1 - e^{-i/\tau}) \]

\[ \rightarrow V_{in} e^{-T_s/2} \ll \Delta \quad \text{or} \quad \tau << \frac{T_s}{2 \ln \left(\frac{V_{in}}{\Delta}\right)} \]

Worst Case: \( V_{in} = V_{FS} \)

\[ \tau << \frac{1}{2 \ln \left(\frac{2B}{1}\right)} \Rightarrow \frac{1}{B} \]

\[ R << \frac{1}{2f_r C \ln \left(\frac{2B}{1}\right)} \Rightarrow \frac{0.72}{B f_r C} \]

Example:

\( B = 14, \quad C = 13pF, \quad f_s = 100MHz \)

\( T_s / \tau \gg 19.4 \), or \( 10 \tau \ll T_s / 2 \rightarrow R \ll 40 \Omega \)

Switch On-Resistance

Switch \( \rightarrow \) MOS operating in triode mode:

\[ I_{D\text{,triode}} = \mu C_m \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}, \quad \frac{1}{R_{ON}} \equiv \frac{dI_{D\text{,triode}}}{dV_{DS}} \bigg|_{V_{in}=0} \]

\[ R_{ON} = \frac{1}{\mu C_m \frac{W}{L} (V_{GS} - V_{TH})} = \frac{1}{\mu C_m \frac{W}{L} (V_{DD} - V_{TH} - V_{in})} \]

Let us call \( R \) @ \( V_{in}=0 \) \( R_o \) then \( R_{o} = \frac{1}{\mu C_m \frac{W}{L} (V_{DD} - V_{TH})} \)

\[ R_{ON} = \frac{R_o}{V_{in} - V_{TH}} \]

\[ V_{GS} = V_{DD} - V_{in} \]

\[ \phi_1 \rightarrow V_{DD} \]
Sampling Distortion

Simulated 10-Bit ADC &

\[ T/2 = 5 \tau \]

\[ V_{DD} - V_{th} = 2V \]
\[ V_{FS} = 1V \]

Sampling Switch modeled:

\[ V_{out} = \left( 1 - e^{-\frac{2\pi}{V_{DD} - V_{th}}} \right) \left( \frac{V_i}{V_{scale}} \right) \]

\[ \Rightarrow \text{Results in} \]

HD2 = -41dBFS &
HD3 = -51.4dBFS

Doubling sampling time (or \( \frac{1}{2} \) time constant)

Results in:

HD2 improved from -41dBFS to -70dBFS \(~30dB\)
HD3 improved from -51.4dBFS to -76.3dBFS \(~25dB\)

Allowing enough time for the sampling network settling \( \Rightarrow \)

Reduces distortion due to switch R non-linear behavior to a tolerable level

10bit ADC  \[ T/2 = 10 \tau \]

\[ V_{DD} - V_{th} = 2V \]
\[ V_{FS} = 1V \]
Sampling Distortion

Effect of Supply Voltage

- Effect of higher supply voltage on sampling distortion
  - HD3 decrease by \((V_{DD1}/V_{DD2})^2\)
  - HD2 decrease by \((V_{DD1}/V_{DD2})\)

SFDR → sensitive to sampling distortion - improve linearity by:
- Larger \(V_{DD}/V_{FS}\)
- Higher sampling bandwidth

Solutions:
- Overdesign → Larger switches
- Increased nonlinear \(S & D\) junction cap.
- Maximize \(V_{DD}/V_{FS}\)
- Decreased dynamic range if \(V_{DD}\) const.
- Complementary switch
- Constant & max. \(V_{GS} \neq f(V_m)\)

10bit ADC & \(T_s/2 = 5\tau\)
\(V_{DD} - V_{th} = 2V\) \(V_{FS} = 1V\)

10bit ADC & \(T_s/2 = 5\tau\)
\(V_{DD} - V_{th} = 4V\) \(V_{FS} = 1V\)
Practical Sampling
Summary So Far!

- \( kT/C \) noise
  \[
  C \geq 12kT \frac{2B}{V_{FS}^2}
  \]
- Finite \( R_{sw} \) \( \rightarrow \) limited bandwidth
  \[
  R \ll \frac{0.72}{Bf_sC}
  \]
- \( g_{sw} = f(V_{in}) \) \( \rightarrow \) distortion
  \[
  g_{ON} = g_o \left( 1 - \frac{V_{in}}{V_{DD} - V_{th}} \right)
  \]
  for
  \[
  g_o = \frac{\mu C_{ox}W}{L}(V_{DD} - V_{th})
  \]

Sampling: Use of Complementary Switches

- Complementary n & p switch advantages:
  - Increase in the overall conductance
  - Linearize the switch conductance for the range \([V_{th}^p] < V_{in} < V_{dd} - [V_{th}^n] \)
Complementary Switch Issues
Supply Voltage Evolution

- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly


Complementary Switch
Effect of Supply Voltage Scaling

- As supply voltage scales down input voltage range for constant $g_0$ shrinks
  $\Rightarrow$ Complementary switch not effective when $V_{DD}$ becomes comparable to $2V_{in}$
Boosted & Constant $V_{GS}$ Sampling

- Gate voltage $V_{GS} =$ low
  - Device off
  - Beware of signal feedthrough due to parasitic capacitors

- Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
  - Switch overdrive voltage independent of signal level
  - Error due to finite $R_{ON}$ linear (to 1st order)
  - Lower $R_{on} \rightarrow$ lower time constant

Constant $V_{GS}$ Sampling

- Boosted clock
- Input signal (voltage at the switch input terminal)
**Constant $V_{GS}$ Sampling Circuit**

This Example: All device sizes: 10μ/0.35μ
All capacitor size: 1pF (except for Chold)
Note: Each critical switch requires a separate clock booster

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**Clock Voltage Doubler**

a) Start-up

b) Next clock phase
Clock Voltage Doubler

- Both C1 & C2 charged to VDD after one clock cycle.
- Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD.

C1

M1

M2

Triode

\( 3V \rightarrow 6V \)

\( (6V-V_{th M2}) \rightarrow (3V-V_{th M2}) \rightarrow 3V \)

Acquires charge

C2

PB

\( 0 \) – 3V

\( 3V \rightarrow 0 \)

c) Next clock phase

Clock period: 100ns

\( *R1 \ & \ R2 = 1 \text{GOhm} \)

*dummy resistors added for simulation only
Constant $V_{GS}$ Sampler: $\Phi$ Low

- Sampling switch M11 is OFF
- C3 charged to $\sim$VDD

Constant $V_{GS}$ Sampler: $\Phi$ High

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant $V_{GS} = VDD$
Constant $V_{GS}$ Sampling

Boosted Clock Sampling
Complete Circuit

Remaining issues:
- $V_{GS}$ constant only for $V_{in} < V_{out}$
- Nonlinearity due to $V_{th}$ dependence of M11 on body-source voltage

Advanced Clock Boosting Technique


• clk → low
  - Capacitors C1a & C1b → charged to VDD
  - MS → off
  - Hold mode
Advanced Clock Boosting Technique

• clk → high
  – Top plate of C1a & C1b connected to gate of sampling switch
  – Bottom plate of C1a connected to \( V_{IN} \)
  – Bottom plate of C1b connected to \( V_{OUT} \)
  – VGS & VGD of MS both @ VDD & ac signal on G of MS → average of \( V_{IN} \) & \( V_{OUT} \)


• Gate tracks average of input and output, reduces effect of I-R drop at high frequencies
• Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
• Reported measured SFDR = 76.5dB at \( f_s = 200\)MHz
Constant Conductance Switch

Constant Conductance Switch

M2 $\rightarrow$ Constant current
$\rightarrow$ constant $g_{ds}$

M1 $\rightarrow$ replica of M2
& same VGS
as M2
$\rightarrow$ M1 also
constant $g_{ds}$

- Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC
- Also, opamp common-mode compliance for full input range required

Switch Off-Mode Feedthrough Cancellation

Practical Sampling

\[ V_i \xrightarrow{\phi_1} V_o \]

- \( R_{sw} = f(V_i) \rightarrow \text{distortion} \)
- Switch charge injection & clock feedthrough

Sampling Switch Charge Injection & Clock Feedthrough

Switching from Track to Hold

- First assume \( V_i \) is a DC voltage
- When switch turns off \( \rightarrow \) offset voltage induced on \( C_s \)
- Why?
Sampling
Switch Charge Injection

MOS xtor operating in triode region
Cross section view

Distributed channel resistance &
gate & junction capacitances

- Channel $\rightarrow$ distributed RC network formed between G, S, and D
- Channel to substrate junction capacitance $\rightarrow$ distributed & voltage dependant
- Drain/Source junction capacitors to substrate $\rightarrow$ voltage dependant
- Over-lap capacitance $C_{ov} = L_D W x C_{ox}$ associated with G-S, G-D overlap

Switch Charge Injection
Slow Clock

- Slow clock $\rightarrow$ clock fall time $>>$ device speed
  $\Rightarrow$ During the period ($t_{to}$ to $t_{off}$) current in channel discharges channel charge into low impedance signal source
- Only source of error $\rightarrow$ Clock feedthrough from $C_{ov}$ to $C_s$
Switch Clock Feedthrough
Slow Clock

\[ \Delta V = -\frac{C_{sw}}{C_{sw} + C_s} (V_i + V_{th} - V_L) \]

where \( \epsilon = \frac{C_{sw}}{C_s} \)

\[ V_o = \frac{C_{sw}}{V_i - (V_i + V_{th} - V_L)} = \frac{C_{sw}}{C_s} (V_{th} - V_L) \]

Switch Charge Injection & Clock Feedthrough
Slow Clock- Example

\[ C_{sw} = 0.1 fF / \mu \quad C_s = 9 fF / \mu \quad V_a = 0.4 V \quad V_L = 0 \]

\[ \epsilon = -\frac{C_{sw}}{C_s} = -10 \mu \times 0.1 fF / \mu = -1.1 \% \]

Allowing \( \epsilon = 1/2 \text{LSB} \) → ADC resolution ≈ 9 bit

\[ V_o = \frac{C_{sw}}{C_s} (V_{th} - V_L) = -0.4 mV \]