• Switched-capacitor filters (continued)
  – DDI integrators
  – LDI integrators
    • Effect of parasitic capacitance
    • Bottom-plate integrator topology
  – Switched-capacitor resonators
  – Bandpass S.C. filters
  – Lowpass S.C. filters
  – Switched-capacitor filter design considerations
    • Termination implementation
    • Transmission zero implementation
    • Effect of non-idealities
  – Switched-capacitor filters utilizing double sampling technique

DDI Switched-Capacitor Integrator

\[
\frac{V_o}{V_{in}}(z) = -\frac{C_s}{C_f} \times \frac{z^{-1}}{1 - e^{-jT}} = \frac{C_s}{C_f} \times \frac{1}{1 - z}, \quad z = e^{jT}
\]

\[
= \frac{C_s}{C_f} \times \frac{1}{1 - e^{-jT}} = \frac{C_s}{C_f} \times \frac{e^{-jT/2}}{e^{-jT/2} - e^{jT/2}} \quad \text{since: } \sin \alpha = \frac{e^{j\alpha} - e^{-j\alpha}}{2j}
\]

\[
= -\frac{C_s}{C_f} \times e^{-jT/2} \times \frac{1}{2\sin(\omega f / 2)}
\]

\[
= -\frac{C_s}{C_f} \times \frac{\omega f / 2}{\sin(\omega f / 2)} \times e^{-j\omega f / 2}
\]

Ideal Integrator  Magnitude Error  Phase Error
DDI Switched-Capacitor Integrator

Example: Mag. & phase error for:

1. $f_s/f = 1/12 \rightarrow$ Mag. error = 1% or 0.1dB
   Phase error = 15 degree
   $Q_{int} = 3.8$

2. $f_s/f = 1/32 \rightarrow$ Mag. error = 0.16% or 0.014dB
   Phase error = 5.6 degree
   $Q_{int} = -10.2$

Example: 5th Order Elliptic Filter

- Ideal Pole
- Ideal Zero
- DDI Pole
- DDI Zero

Example:
- 5th Order Elliptic Filter
  Singularity pushed towards RHP due to integrator excess phase
Switched Capacitor Filter
Build with DDI Integrator

$|H(j\omega)|$

Passband
Peaking
SC DDI based
Filter
Zeros lost!

Continuous-Time
Prototype

$\frac{f_s}{2}$

$f_s$

$2f_s$

$f$

Switched-Capacitor Integrator
Output Sampled on $\phi_2$

Sample output $\frac{1}{2}$ clock cycle earlier
→ Sample output on $\phi_2$
\[
\phi_1 \rightarrow Q_i[(n-1)T] = C_i V_i[(n-1)T] \quad , \quad Q_i[(n-1)T] = Q_o[(n-3/2)T] \\
\phi_2 \rightarrow Q_i[(n-1/2)T] = 0 \quad , \quad Q_i[(n-1/2)T] = Q_o[(n-3/2)T] + Q_i[(n-1)T] \\
\phi_1 \rightarrow Q_i[nT] = C_i V_i[nT] \quad , \quad Q_i[nT] = Q_o[(n-1)T] + Q_i[(n-1)T] \\
\phi_2 \rightarrow Q_i[(n+1/2)T] = 0 \quad , \quad Q_o[(n+1/2)T] = Q_o[(n-1/2)T] + Q_i[nT]
\]

Using the z operator rules:

\[
V_{o2} = \frac{-Q_i}{C_i} V_i \rightarrow C_i V_{o2} z^{1/2} - C_i V_i = \frac{-C_o}{C_i} \times \frac{z^{-1/2}}{1-z^{-1}} V_{in}
\]
LDI Switched-Capacitor Integrator

LDI (Lossless Discrete Integrator) → same as DDI but output is sampled vs clock cycle earlier

\[
\frac{V_{o2}(z)}{V_{in}} = -\frac{C_2}{C_1} \times \frac{z^{-1/2}}{1-z^{-1}}, \quad z = e^{j\omega T}
\]

\[
= -\frac{C_2}{C_1} \times \frac{e^{-j\omega T/2}}{1-e^{-j\omega T/2}} = \frac{C_2}{C_1} \times \frac{e^{-j\omega T/2} - e^{j\omega T/2}}{e^{-j\omega T/2} - e^{j\omega T/2}}
\]

\[
= -\frac{jC_2}{C_1} \times \frac{1}{2\sin(\omega T/2)}
\]

No Phase Error!
For signals at frequencies \(<<\) sampling freq. → Magnitude error negligible

Switched-Capacitor Filter
Built with LDI Integrators

\[|H(j\omega)|\]
Zeros Preserved

- \(f_s/2\)
- \(f_s\)
- \(2f_s\)
- \(f\)
Switched-Capacitor Integrator
Parasitic Capacitor Sensitivity

Effect of parasitic capacitors:

1. $C_{p3}$ — driven by opamp o.k.
2. $C_{p2}$ — at opamp virtual gnd o.k.
3. $C_{p1}$ — Charges to $V_{in}$ & discharges into $C_I$,
   
   $= C_{p1}$ includes the MOS switch junction capacitors which are voltage
   dependent, not only affects $C$ ratios but results in non-linearities

$\Rightarrow$ Problem parasitic capacitor sensitivity

Parasitic Insensitive
Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. $\Rightarrow C_{p1} \Rightarrow$ rearrange circuit so that $C_{p1}$ does not
charge/discharge

$\phi_1 = 1 \Rightarrow C_{p1}$ grounded

$\phi_2 = 1 \Rightarrow C_{p1}$ at virtual ground

Solution: Bottom plate capacitor integrator
Bottom Plate Switched-Capacitor Integrator

Note:
Different delay from Vi+ & Vi- to either output
⇒ Special attention needed for input/output connections to ensure LDI realization

<table>
<thead>
<tr>
<th></th>
<th>Vo1</th>
<th>Vo2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vi+ on φ₁</td>
<td>$\frac{C_S}{C_I} \frac{z^{-1}}{1-z^{-1}}$</td>
<td>$\frac{C_S}{C_I} \frac{z^{-1/2}}{1-z^{-1}}$</td>
</tr>
<tr>
<td>Vi- on φ₂</td>
<td>$\frac{C_S}{C_I} \frac{z^{-1/2}}{1-z^{-1}}$</td>
<td>$\frac{C_S}{C_I} \frac{1}{1-z^{-1}}$</td>
</tr>
</tbody>
</table>

Bottom Plate Switched-Capacitor Integrator
z-Transform Model
LDI Switched-Capacitor Ladder Filter

To test whether LDI or DDI → Need to examine delay around the integrator loop

**Delay around integrator loop is** \((z^{-1/2} \cdot z^{+1/2} = 1)\) → **LDI function**

Switched-Capacitor LDI Resonator

**Resonator Signal Flowgraph**

\[
\omega_1 = \frac{1}{R_{eq} C_2} = f_s \times \frac{C_1}{C_2}
\]

\[
\omega_2 = \frac{1}{R_{eq} C_4} = f_s \times \frac{C_3}{C_4}
\]
Fully Differential Switched-Capacitor Resonator

- Note: Two sets of S.C. bottom plate networks for each differential integrator

Switched-Capacitor LDI Bandpass Filter Utilizing Continuous-Time Termination

Feedback in the amount of \(-1/Q\) provided from \(V_{o2}\) to \(V_{o1}\) via the addition of capacitor \(C_Q\)

\[
\omega_0 = f_s \cdot \frac{C_1}{C_J} = f_s \cdot \frac{C_1}{C_2} \\
Q = \frac{C_2}{C_Q}
\]
Example: 2\textsuperscript{nd} Order S.C. Bandpass Filter
s-Plane versus z-Plane

Switched-Capacitor LDI Bandpass Filter
Continuous-Time Termination

\[ f_0 = \frac{1}{2\pi f_s} \times \frac{C_1}{C_2} \]
\[ \Delta f = \frac{f_0}{Q} \]
\[ \Delta f = \frac{1}{2\pi f_s} \times \frac{C_1 C Q}{C_2^2} \]

Both \( f_0 \) and \( \Delta f \) accurately determined by cap ratios & clock frequency.
Fifth Order All-Pole LDI Low-Pass Ladder Filter
Complex Conjugate Terminations

- Complex conjugate terminations (alternate phase switching)


Fifth-Order All-Pole Low-Pass Ladder Filter
Termination Implementation

Sixth-Order Elliptic LDI Bandpass Filter


Use of T-Network

High Q filter \(\rightarrow\) large cap. ratio for Q & transmission zero implementation
To reduce large ratios required \(\rightarrow\) T-networks utilized

Sixth Order Elliptic Bandpass Filter Utilizing T-Network

- T-networks utilized for:
  - Q implementation
  - Transmission zero implementation


Effect of Opamp Nonidealities on Switched Capacitor Filter Behavior

- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity - usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)
Effect of Opamp Non-Idealities
Finite DC Gain

\[ H(s) \approx -f_s \frac{C_s}{C_f} \frac{1}{s + f_s \frac{C_s}{C_f} \times \frac{1}{a}} \]

\[ H(s) \approx \frac{-\omega_0}{s + \omega_0 \times \frac{1}{a}} \]

\[ \Rightarrow Q_{intg} \approx a \]

• Finite DC gain same effect in S.C. filters as for C.T. filters
• If DC gain not high enough → lowing of overall Q & droop in passband

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

Assumption-
Opamp → does not slew (will be revisited)
Opamp has one pole only → exponential settling

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

\[ H_{\text{actual}}(Z) \approx H_{\text{ideal}}(Z) \left[ 1 - e^{-k} + e^{-k} \frac{C_l}{C_l + C_s} Z^{-1} \right] \]

where \( k = \pi \times \frac{C_l}{C_l + C_s} \frac{f_t}{f_s} \)

\( f_t \to \text{Opamp unity-gain frequency} \), \( f_s \to \text{Clock frequency} \)


---

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

Example:
For 1dB magnitude response deviation:
1. \( f_c/f_s = 1/12 \)
   \( f_c/f_t = 0.04 \) → \( f_t > 25 f_c \)
2. \( f_c/f_s = 1/32 \)
   \( f_c/f_t = 0.022 \) → \( f_t > 45 f_c \)
3. Cont. Time
   \( f_c/f_t = 1/700 \) → \( f_t > 700 f_c \)

Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%

1. \( f_c/f_s = 1/32 \)
   \( f_c/f_s \approx 0.028 \)
   \( f_t > 36f_c \)

2. \( f_c/f_s = 1/12 \)
   \( f_c/f_s \approx 0.046 \)
   \( f_t > 22f_c \)

3. Active RC
   \( f_c/f_s \approx 0.008 \)
   \( f_t > 125f_c \)


Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  → Results in negative intg. Q & thus increases overall Q → results in peaking in the passband of interest

- For given filter requirements, opamp bandwidth requirements much less stringent for S.C. filters compared to cont. time filters
  → Lower power dissipation for S.C. filters (at low freq.s only since other nonidealities dominate at high freq.s)

- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  – Since cont. time filters are usually tuned → tuning accounts for frequency deviation
  – S.C. filters are untuned and thus frequency shift could cause problems particularly for narrow-band filters
Effect of Opamp Nonidealities on Switched-Capacitor Filter Performance

- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity- usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)

What is Slewing?

Assumption:
Integrator opamp is a simple class A transconductance type differential pair with fixed tail current, \( Iss=const.\)
What is Slewing?

\[ |V_{Cs}| > V_{\text{max}} \Rightarrow \text{Output current constant } I_o = \frac{I_{ss}}{2} \text{ or } -\frac{I_{ss}}{2} \]
\[ \Rightarrow \text{Constant current charging/discharging } C_s: V_o \text{ ramps down/up } \Rightarrow \text{Slewing} \]

After \( V_{Cs} \) is discharged enough to have:
\[ |V_{Cs}| < V_{\text{max}} \Rightarrow I_o = g_m \cdot V_{Cs} \Rightarrow \text{Output} \Rightarrow \text{Exponential or over/under-shoot settling} \]
Ideal Switched-Capacitor Output Waveform

Slew Limited Switched-Capacitor Integrator
Output Slewing & Settling
Distortion Induced by Finite Slew Rate of the Opamp


Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)
  
  → For high-linearity need to have either high slew rate or non-slewing opamp

\[ HD_k = \frac{V_o}{S_{rT_s}} \left(\sin \frac{\alpha \pi}{2}\right)^2 \frac{\pi k}{\left(k^2 - 4\right)} \]

\[ \rightarrow HD_3 = \frac{V_o}{S_{rT_s}} \left(\sin \frac{\alpha \pi}{2}\right)^2 \frac{8}{15\pi} \quad \text{for} \quad f_o << f_s \rightarrow HD_3 = \frac{8\pi V_o f_0^2}{75S_f f_s} \]

Example:
Slew Related Harmonic Distortion

\[ HD_3 = \frac{V_o}{S_r T_s} 8 \left( \sin \left( \frac{\alpha T_s}{2} \right) \right)^2 \]

\[ HD_3 \approx \frac{8\pi V_o}{15S_r} \frac{f_o^2}{f_s} \]


Distortion Induced by Opamp Finite Slew Rate

Example

\[ HD_3 (dB) \]

\[ f / f_s = 1/32 \]

\[ V_o = 4V \]

\[ f / f_s = 1/12 \]

\[ V_o = 2V \]

\[ f / f_s = 1/32 \]

\[ V_o = 4V \]

\[ f / f_s = 1/12 \]

\[ V_o = 2V \]
Distortion Induced by Finite Slew Rate of the Opamp

• Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  → Can reduce slew limited non-linearities by using an amplifier with a higher slew rate only for the last stage
  → Can reduce slew limited non-linearities by using class A/B amplifiers
    • Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion in S.C. filters

• In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario

At the instant $C_s$ connects to input of opamp ($t=0+$)
→ Opamp not yet active at $t=0+$ due to finite opamp bandwidth → delay
→ Feedforward path from input to output generates a voltage spike at the output with polarity opposite to final $V_o$ step- spike magnitude function of $C_i, C_L, C_s$
→ Spike increases slewing period
→ Eventually, opamp becomes active - starts slewing followed by subsequent settling
Switched-Capacitor Circuit
Opamp not Active @ \( t=0^+ \)

**Charge sharing:**
\[ C_s V_{CS}^{t=0^-} = V_{CI}^{t=0^-} (C_s + C_{eq}) \]

where
\[ C_{eq} = \frac{C_I C_L}{C_I + C_L} \]

\[ \Delta V_{out}^{t=0^+} = V_{CS}^{t=0^-} \frac{C_I}{C_I + C_L} = V_{CI}^{t=0^-} \frac{C_s + C_{eq}}{C_I + C_L} \]

Assuming \( C_L \ll C_I \ll C_s \rightarrow C_{eq} \approx C_L \rightarrow C_s V_{CS}^{t=0^-} \approx V_{CS}^{t=0^-} (C_s + C_L) \rightarrow V_{CI}^{t=0^-} \approx V_{CI}^{t=0^-} \]

\[ \Rightarrow \Delta V_{out}^{t=0^+} \approx \frac{C_I}{C_I + C_L} \approx \frac{C_s}{C_I} \]

Note that
\[ \Delta V_{out}^{t=0^+} \approx \frac{C_I}{C_I + C_L} \]

Notice that if \( C_L \) is large \( \rightarrow \) some of the charge stored on \( C_s \) is lost prior to opamp becoming effective \( \rightarrow \) operation loses accuracy

**Charge sharing:**
\[ C_s V_{CS}^{t=0^-} = V_{CI}^{t=0^-} (C_s + C_{eq}) \]

where
\[ C_{eq} = \frac{C_I C_L}{C_I + C_L} \]

\[ V_{CS}^{t=0^-} = V_{CI}^{t=0^-} \frac{C_s}{C_s + C_{eq}} = V_{CI}^{t=0^-} \frac{C_s}{C_s + \frac{C_I C_L}{C_I + C_L}} \]

\( \rightarrow \) Partly responsible for S.C. filters only good for low-frequency applications
More Realistic S.C. Slew Scenario


Effect of Opamp Nonidealities on Switched Capacitor Filter Behavior

- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity - usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)
Sources of Noise in Switched-Capacitor Filters

- Opamp Noise
  - Thermal noise
  - 1/f (flicker) noise
- Thermal noise associated with the switching process (kT/C)
  - Same as continuous-time filters
- Precaution regarding aliasing of noise required

Extending the Maximum Achievable Critical Frequency of Switched-Capacitor Filters

Consider a switched-capacitor resonator:

Regular sampling:
Each opamp is busy settling only during one of the two clock phases

→ Idle during the other clock phase

Note: During φ1 both opamps are idle
Switched-Capacitor Resonator Using Double-Sampling

Double-sampling:

- 2nd set of switches & sampling caps added to all integrators

- While one set of switches/caps sampling the other set transfers charge into the intg. cap

- Opamps busy during both clock phases

  - Effective sampling freq. twice the clock freq. while opamp bandwidth requirement remains the same

Double-Sampling Issues

Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
- Mismatch in sampling caps.

→ Results in parasitic passbands

Sixth Order Bandpass Filter Signal Flowgraph

Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

- Cont. time termination (Q) implementation
- Folded-Cascode opamp with $f_c = 100MHz$ used
- Center freq. 3.1MHz (Measured error >1%), filter Q=55
- Clock freq. 12.83MHz $\rightarrow$ effective oversampling ratio 8.27
- Measured dynamic range 46dB (IM3=1%)

Switched-Capacitor Filter Application
Example: Voice-Band CODEC (Coder-Decoder) Chip


CODEC Transmit Path
Lowpass Filter Frequency Response
CODEC Transmit Path
Highpass Filter

Note: \( f_s = 8 \text{kHz} \)

Low Q bandpass (Q<1) filter shape → Implemented with lowpass followed by highpass
CODEC Transmit Path  
Clocking Scheme

First filter (1st order RC type) performs anti-aliasing for the next S.C. biquad

The first 2 stage filters form 3rd order elliptic with corner frequency @ 32kHz → Anti-aliasing for the next S.C. lowpass filter with 3.4kHz corner freq.

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency → Ease of anti-aliasing

---

SC Filter Summary

- Pole and zero frequencies proportional to
  - Sampling frequency $f_s$
  - Capacitor ratios
  - High accuracy and stability in response
  - Long time constants realizable without large R, C
- Compatible with transconductance amplifiers
  - Reduced circuit complexity, power dissipation
- Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)

⚠️ Issue: Sampled-data filters → require anti-aliasing prefiltering
Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects:

- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Opamp finite slew rate
- Clock feedthru & switch charge injection
- Switch+ sampling cap. finite time-constant

→ Limited switched-capacitor filter performance frequency range

Summary
Filter Performance versus Filter Topology

<table>
<thead>
<tr>
<th></th>
<th>Max. Usable Bandwidth</th>
<th>SNDR</th>
<th>Freq. Tolerance w/o Tuning</th>
<th>Freq. Tolerance + Tuning</th>
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</thead>
<tbody>
<tr>
<td>Opamp-RC</td>
<td>~10MHz</td>
<td>60-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-C</td>
<td>~5MHz</td>
<td>40-60dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-RC</td>
<td>~5MHz</td>
<td>50-90dB</td>
<td>+30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Gm-C</td>
<td>~100MHz</td>
<td>40-70dB</td>
<td>+40-60%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Switched Capacitor</td>
<td>~10MHz</td>
<td>40-90dB</td>
<td>&lt;1%</td>
<td></td>
</tr>
</tbody>
</table>
Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do S.C. integrators map frequencies?

\[
H_{s.c.}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}
\]

\[
= -\frac{C_s}{C_{int}} \frac{1}{2 j \sin \pi f T}
\]

CT – SC Integrator Comparison

CT Integrator

\[
H_{RC}(s) = \frac{1}{s \tau} = -\frac{1}{2 \pi f_s j \tau}
\]

SC Integrator

\[
H_{SC}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}
\]

\[
= -\frac{C_s}{C_{int}} \frac{1}{2 j \sin \pi f_{SC} T_s}
\]

Identical time constants:

\[
\tau = RC = \frac{C_{int}}{f_s C_s}
\]

Set: \( H_{RC}(f_{RC}) = H_{SC}(f_{SC}) \)

\[
f_{RC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right)
\]
LDI Integration

\[ f_{RC} = \frac{f_s}{\pi} \sin \left( \pi \frac{f_{SC}}{f_s} \right) \]

- “RC” frequencies up to \( f_s / \pi \) map to physical (real) “SC” frequencies
- Frequencies above \( f_s / \pi \) do not map to physical frequencies
- Mapping is symmetric about \( f_s / 2 \) (aliasing)
- “Accurate” only for \( f_{RC} \ll f_s \)

Material Covered in EE247

Where are We?

- Filters
  - Continuous-time filters
    - Biquads & ladder type filters
    - Opamp-RC, Opamp-MOSFET-C, gm-C filters
    - Automatic frequency tuning
  - Switched capacitor (SC) filters
- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Pipeline ADCs,…..
    - Oversampled converters
    - Self-calibration techniques
- Systems utilizing analog/digital interfaces