EE247
Lecture 17

• Administrative issues
  ▪ Midterm exam postponed to **Thurs. Oct. 28th**
    o You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    o No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    o Midterm includes material covered to **end of lecture 14**

EE247
Lecture 17

ADC Converters
  – Sampling (continued)
    • Sampling switch considerations
      – Clock voltage boosters
      – Sampling switch charge injection & clock feedthrough
        • Complementary switch
        • Use of dummy device
        • Bottom-plate switching
  – Track & hold
    • T/H circuits
    • T/H combined with summing/difference function
    • T/H circuit incorporating gain & offset cancellation
    • T/H aperture uncertainty
Practical Sampling Summary So Far!

- $kT/C$ noise
  \[ C \geq 12kT \frac{2^{2B}}{V_{FS}^2} \]
- Finite $R_{sw} \rightarrow$ limited bandwidth
  \[ R \ll \frac{0.72}{Bf_sC} \]
- $g_{sw} = f(V_{in}) \rightarrow$ distortion
  \[ g_{ON} = g_o \left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right) \quad \text{for} \quad g_o = \mu C_{ox} \frac{W}{L} (V_{DD} - V_{th}) \]
- Allowing long enough settling time $\rightarrow$ reduce distortion due to switch non-linear behavior

Constant V$_{GS}$ Sampling Circuit

This Example: All device sizes: $W/L=10\mu/0.35\mu$
All capacitor size: 1pF (except for Chold)
Note: Each critical switch requires a separate clock booster

Clock Voltage Doubler

Clock period: 100ns

R1 & R2 = 1GΩm

dummy resistors added for simulation only

Constant $V_{GS}$ Sampler: $\Phi$ Low

• Sampling switch M11 is OFF

• C3 charged to ~VDD
Constant $V_{GS}$ Sampler: $\Phi$ High

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant $V_{GS} = VDD$
- Mission accomplished!?
Constant $V_{GS}$ Sampling?

- During the time period: $V_{in} < V_{out}$
  - $V_{GS} = \text{constant} = V_{DD}$
  - Larger $V_{GS} - V_{th}$ compared to no boost
  - $V_{GS} = \text{cte}$ and not a function of input voltage
  - Significant linearity improvement

- During the time period: $V_{in} > V_{out}$:
  - $V_{GS} = V_{DD} - IR$
  - Larger $V_{GS} - V_{th}$ compared to no boost
  - $V_{GS}$ is a function of $IR$ and hence input voltage
  - Linearity improvement not as pronounced as for $V_{in} < V_{out}$
Boosted Clock Sampling Design Considerations

Choice of value for C3:

• C3 too large ⇒ large charging current ⇒ large dynamic power dissipation

• C3 too small ⇒
  \[(\text{V}_{\text{gate-Vs}})_{\text{M11}} = \frac{\text{VDD}.C3}{(C3+Cx)}\]
  ⇒ Loss of \( V_{\text{GS}_{\text{M11}}} \) due to low ratio of \( C3/Cx \)
  Cx includes \( C_{\text{GS}} \) of M11 plus all other parasitics caps….


Boosted Clock Sampling Design Considerations

• Reliability issues:
  – Avoid having any of the G-S and G-D, and D-S terminal voltages for ALL circuit devices exceed the maximum \( V_{\text{DD}} \) prescribed by the SI processing firm.

  – In particular, the thin MOS device gate oxide could gradually sustain damage through getting exposed to higher than prescribed voltage.
Boosted Clock Sampling
Complete Circuit

- $V_{GS}$ constant only for $V_{in} < V_{out}$
- Nonlinearity due to $V_{th}$ dependence of $M11$ on body-source voltage


Advanced Clock Boosting Technique


Two floating voltages sources generated and connected to Gate and S & D
Advanced Clock Boosting Technique

- **clk → low**
  - Capacitors C1a & C1b → charged to VDD
  - MS → off
  - Hold mode

- **clk → high**
  - Top plate of C1a & C1b connected to gate of sampling switch
  - Bottom plate of C1a connected to \( V_{IN} \)
  - Bottom plate of C1b connected to \( V_{OUT} \)
  - \( V_{GS} \) & \( V_{GD} \) of sampling switch (MS) both @ VDD & ac signal on G of MS
  - average of \( V_{IN} \) & \( V_{OUT} \)
Advanced Clock Boosting Technique

- Gate tracks average of input and output, reduces effect of I-R drop at high frequencies
- Bulk also tracks signal \(\Rightarrow\) reduced body effect (technology used allows connecting bulk to S)
- Reported measured SFDR = 76.5dB at \(f_{in}=200\text{MHz}\)


Constant Conductance Switch

Constant Conductance Switch


M2 → Constant current

M1 → replica of M2 & same VGS as M2 → M1 also → constant current

• Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC

• Also, opamp common-mode compliance for full input range required

Switch Off-Mode Feedthrough Cancellation

High-pass feedthrough paths past an open switch

Feedthrough cancellation with a dummy switch


Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite $R_{sw}$ → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough
Sampling Switch Charge Injection & Clock Feedthrough
Switching from Track to Hold

- First assume $V_i$ is a DC voltage
- When switch turns off → unwanted offset voltage induced on $C_s$
- Why?

Sampling Switch Charge Injection

MOS xtor operating in triode region
Cross section view

- Channel → distributed RC network formed between G, S, and D
- Channel to substrate junction capacitance → distributed & voltage dependant
- Drain/Source junction capacitors to substrate → voltage dependant
- Over-lap capacitance $C_{ov} = L_D W C_{ox}$ associated with G-S & G-D overlap
Switch Charge Injection
Slow Clock

- Slow clock → clock fall time >> device speed
  → During the period \((t \rightarrow t_{off})\) current in channel discharges channel charge into low impedance signal source

- Only source of error → Clock feedthrough from \(C_{ov}\) to \(C_s\)

\[
\Delta V = -\frac{C_{ov}}{C_s + C_{ov}} (V_i + V_{ih} - V_L) \\
\approx -\frac{C_{ov}}{C_s} (V_i + V_{ih} - V_L) \\
V_o = V_i + \Delta V \\
V_o = V_i - \frac{C_{ov}}{C_s} (V_i + V_{ih} - V_L) = V_i \left(1 - \frac{C_{ov}}{C_s} \right) - \frac{C_{ov}}{C_s} (V_{ih} - V_L) \\
V_o = V_i (1 + \varepsilon) + V_{os} \\
\text{where } \varepsilon = -\frac{C_{ov}}{C_i}; \ V_{os} = -\frac{C_{ov}}{C_s} (V_{ih} - V_L)
\]
Switch Charge Injection & Clock Feedthrough

Slow Clock - Example

\[ C_{ov} = 0.1 fF/ \mu \quad C_{ox} = 9 fF/ \mu^2 \quad V_{th} = 0.4 V \quad V_L = 0 \]
\[ \varepsilon = - \frac{C_{ov} \mu_{0.1 fF/ \mu}}{C_s} = -1 \% \]

Allowing \( \varepsilon = 1/2 \)LSB → ADC resolution \(< 9\) bit

\[ V_{os} = - \frac{C_{ov}}{C_s} (V_{th} - V_L) = -0.4 mV \]

Fast Clock

\[ nQ_{ch} \quad n = m \]

• Sudden gate voltage drop → no gate voltage to establish current in channel
  → channel charge has no choice but to escape out towards S & D
Switch Charge Injection & Clock Feedthrough
Fast Clock

Clock Fall-Time $< <$ Device Speed:

$$
\Delta V_o = -\frac{C_{ov}}{C_{ov} + C_s} (V_H - V_L) - \frac{1}{2} \times \frac{Q_{th}}{C_s}
$$

$$
\approx -\frac{C_{ov}}{C_{ov} + C_s} (V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{iH})}{C_s}
$$

where $\varepsilon = \frac{1}{2} \times \frac{W C_{ox} L}{C_s}$

$$
V_{ox} = -\frac{C_{ox}}{C_s} (V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{iH})}{C_s}
$$

- For simplicity it is assumed channel charge divided equally between S & D
- Source of error $\rightarrow$ channel charge transfer + clock feedthrough via $C_{ov}$ to $C_s$

Switch Charge Injection & Clock Feedthrough
Fast Clock - Example

$$
C_{ov} = 0.1 \mu F, \ C_{ox} = 9 \mu F, \ V_{th} = 0.4 V, \ V_{DD} = 1.8 V, \ V_L = 0
$$

$$
\varepsilon = 1/2 \times \frac{W L C_{ox}}{C_s} = \frac{10 \mu m \times 0.18 \mu m \times 9 \mu F}{1 \mu F} = 1.6\% \rightarrow \sim 5\ -\ bit
$$

$$
V_{ox} = -\frac{C_{ox}}{C_s} (V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{iH})}{C_s} = -1.8 mV - 14.6 mV = -16.4 mV
$$
Switch Charge Injection & Clock Feedthrough Example-Summary

Error function of:
- Clock fall time
- Input voltage level
- Source impedance
- Sampling capacitance size
- Switch size

Clock fall/rise should be controlled not to be faster (sharper) than necessary

Switch Charge Injection Error Reduction

- How do we reduce the error?
  - Reduce switch size to reduce channel charge?

\[ \Delta V_s = \frac{-I Q_{th}}{2 C_s} \]

\[ \tau = R_{ON} C_s = \frac{2 C_s}{\mu C_{ox}(V_{GS} - V_{th})} \]

\( \text{(note: } T_e = k \tau) \)

Consider the figure of merit (FOM):

\[ FOM = \frac{I}{\tau \times \Delta V_s} \approx \frac{\mu C_{ox} W}{L (V_{GS} - V_{th})} \times 2 \times \frac{C_s}{W C_{ox} L ((V_H - V_L - V_{th}) \times C_s)} \]

\[ \Rightarrow FOM \propto \mu / L^2 \]

- Reducing switch size increases \( \tau \) \( \rightarrow \) increased distortion \( \rightarrow \) not a viable solution
- Small \( \tau \) and small \( \Delta V \) \( \rightarrow \) use minimum channel length (mandated by technology)
- For a given technology \( \tau \times \Delta V \) \( \approx \) constant
Sampling Switch Charge Injection & Clock Feedthrough

**Summary**

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Channel charge injection
  - Clock feedthrough to $C_s$ via $C_{ov}$

- Issues due to charge injection & clock feedthrough:
  - DC offset induced on hold $C$
  - Input dependant error voltage $\rightarrow$ distortion

- Solutions:
  - Slowing down clock edges as much as possible
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?

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Switch Charge Injection & Clock Feedthrough

**Complementary Switch**

- In slow clock case if area of n & p devices & widths are equal ($W_n = W_p$) $\rightarrow$ effect of overlap capacitor for n & p devices to first order cancel (cancellation accuracy depends on matching of n & p width and overlap length $L_D$)

- Since in CMOS technologies $\mu_n \approx 2.5\mu_p$ choice of $W_n = W_p$ not optimal from linearity perspective ($W_p > W_n$ preferable)
Switch Charge Injection

Complementary Switch

Fast Clock

\[ Q_{\text{ch-n}} = W_n C_{\text{ox}} L_n (V_H - V_I - V_{\text{ch-n}}) \]

\[ Q_{\text{ch-p}} = W_p C_{\text{ox}} L_p (V_I - V_L - V_{\text{ch-p}}) \]

\[ \Delta V_o \approx \frac{1}{2} \left( \frac{Q_{\text{ch-n}}}{C_i} - \frac{Q_{\text{ch-p}}}{C_i} \right) \]

\[ V_o = V_I (1 + \varepsilon) + V_{\text{offset}} \]

\[ \varepsilon \approx \frac{1}{2} \times \frac{W_n C_{\text{ox}} L_n + W_p C_{\text{ox}} L_p}{C_i} \]

In fast clock case:
- To 1st order, offset due to overlap caps cancelled for equal device width
- Input voltage dependant error worse!

Switch Charge Injection

Dummy Switch

\[ Q_1 \approx \frac{1}{2} Q_{\text{ch-h}}^{M1} + Q_{\text{ov}}^{M1} \]

\[ Q_2 \approx Q_{\text{ch}}^{M2} + 2 Q_{\text{ov}}^{M2} \]

For \( W_{M2} = \frac{1}{2} W_{M1} \) \( \Rightarrow Q_2 = -Q_1 \) \& \( Q_{\text{ov}}^{M1} = 2 Q_{\text{ov}}^{M2} \)
Switch Charge Injection
Dummy Switch

- Dummy switch same L as main switch but half W
- Main device clock goes low, dummy device gate goes high → dummy switch acquires same amount of channel charge main switch needs to lose
- Effective only if exactly half of the charge stored in M1 is transferred to M2 (depends on input/output node impedance) and requires good matching between clock fall/rise

Switch Charge Injection
Dummy Switch

- To guarantee half of charge goes to each side → create the same environment on both sides
  - Add capacitor equal to sampling capacitor to the other side of the switch
  - Add fixed resistor to emulate input resistance of following circuit
- Issues: Degrades sampling bandwidth
**Dummy Switch Effectiveness Test**

- Dummy switch $\Rightarrow W=1/2W_{\text{main}}$
- As $V_{in}$ is increased $V_{c1}-V_{in}$ is decreased $\Rightarrow$ channel charge decreased $\Rightarrow$ less charge injection
- Note large $L_s$ $\Rightarrow$ good device area matching


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**Switch Charge Injection Differential Sampling**

- To $1^{st}$ order, offset terms cancel
- Note gain error $\varepsilon$ still about the same
- Has the advantage of better immunity to noise coupling and cancellation of even order harmonics
Avoiding Switch Charge Injection
Bottom Plate Sampling

- Switches M2 opened slightly earlier compared to M1
  → Injected charge due to turning off M2 is constant since its GS voltage is constant & eliminated when used differentially

- Since $C_s$ bottom plate is already open when M1 is switched off:
  → No signal dependant charge injected on $C_s$

Flip-Around Track & Hold

- Concept based on bottom-plate sampling
Flip-Around T/H-Basic Operation

\( \phi_1 \rightarrow \text{high} \)

Charging C

\( Q_{\phi_1} = V_{IN} \cdot C \)

Note: Opamp has to be stable in unity-gain configuration

Flip-Around T/H-Basic Operation

\( \phi_2 \rightarrow \text{high} \)

Holding

\( Q_{\phi_2} = V_{OUT} \cdot C \)

\( \Rightarrow V_{OUT} = V_{IN} \)
Flip-Around T/H - Timing

S1 opens earlier than S1A
No resistive path from C bottom plate to Gnd  charge can not change "Bottom Plate Sampling"

Charge Injection

- At the instant of transitioning from track to hold mode, some of the charge stored in sampling switch S1 is dumped onto C

- With "Bottom Plate Sampling", only charge injection component due to opening of S1 and is to first-order independent of $v_{IN}$
  - Only a dc offset is added. This dc offset can be removed with a differential architecture
Flip-Around T/H

- S1 is chosen to be an n-channel MOSFET
- Since it always switches the same voltage, it’s on-resistance, $R_{S1}$, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - Typically, S1A is a wide (much lower resistance than S1) & constant $V_{GS}$ switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A’s resistance is negligible $\rightarrow$ delay depends only on S1 resistance
  - S1 resistance is independent of $V_{IN} \rightarrow$ error due to finite time-constant $\rightarrow$ independent of $V_{IN}$
Differential Flip-Around T/H
Choice of Sampling Switch Size

- THD simulated w/o sampling switch boosted clock $\rightarrow -45$dB
- THD simulated with sampling switch boosted clock (see graph)


Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit
During input sampling phase $\rightarrow$ amp outputs shorted together

Differential Flip-Around T/H

- Gain = 1
- Feedback factor = 1 → high operating speed

Differential Flip-Around T/H

Issues: Input Common-Mode Range

- $\Delta V_{in-cm} = V_{out\_com} - V_{sig\_com}$
  - Drawback: Amplifier needs to have large input common-mode compliance

$V_{CM} = 1.5V$

- $1.7V$
- $1.3V$

- $1V$
- $0.5V$

- $1.2V$
- $0.8V$

$\Delta V_{in-cm} = 1 - 1.5 = -0.5V$
Input Common-Mode Cancellation

• Note: Shorting switch M3 added


Input Common-Mode Cancellation

Track mode ($\phi$ high)
$V_{C1}=V_{I1}$, $V_{C2}=V_{I2}$
$V_{C1}=V_{C2}=0$

Hold mode ($\phi$ low)
$V_{C1}+V_{C2}=0$
$V_{C1}-V_{C2}=-(V_{I1}-V_{I2})(C_1/(C_1+C_2))$

→ Input common-mode level removed
Switched-Capacitor Techniques Combining Track & Hold with Other Functions

- T/H + Charge redistribution amplifier
- T/H & Input difference amplifier
- T/H & summing amplifier
- Differential T/H combined with gain stage
- Differential T/H including offset cancellation

T/H + Charge Redistribution Amplifier

Track mode: (S1, S3 → on S2 → off)

\[ V_{C1} = V_{os} - V_{IN} \]
\[ V_{C2} = 0 \]
\[ V_o = V_{os} \]
**T/H + Charge Redistribution Amplifier**

**Hold Mode**

S1 & S3 open
S2 closed

\[ V_{C1} \rightarrow V_{os} \]

\[ \Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN} \]

\[ \Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN} \]

\[ \Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1 \]

\[ \Delta V_{C2} = \frac{C_1}{C_2} V_{C1} = V_{C2} \]

\[ V_o = V_{C2} + V_{os} = \left( \frac{C_1}{C_2} \right) V_{IN} + V_{os} \]

→ Offset NOT cancelled, but not amplified
→ Input-referred offset = \( (C_2/C_1) \times V_{OS} \), & often \( C_2 < C_1 \)

**T/H & Input Difference Amplifier**

**Sample mode:**

(S1, S3 \( \rightarrow \) on S2 \( \rightarrow \) off)

\[ V_{C1} = V_{os} - V_{11} \; , \; V_{C2} = 0 \]

\[ V_o = V_{os} \]
Input Difference Amplifier
Cont’d

Subtract/Amplify mode (S1, S3 \rightarrow \text{off} S2 \rightarrow \text{on})
During previous phase:
\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = 0 \]
\[ V_o = V_{os} \]

\[ V_{C1} = V_{os} - V_{I2} \]
\[ \Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2} \]
\[ \Delta V_{C2} = \left( \frac{C_2}{C_1} \right) \Delta V_{C1} = \left( \frac{C_1}{C_2} \right) (V_{I1} - V_{I2}) \]
\[ V_o = \left( \frac{C_1}{C_2} \right) (V_{I1} - V_{I2}) + V_{os} \]

→ Offset NOT cancelled, but not amplified
→ Input-referred offset = \((C_2/C_1) \times V_{OS}\), \(C_2 < C_1\)

T/H & Summing Amplifier
Sample mode (S1, S3, S5→on S2, S4→off)

\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = V_{os} - V_{I3}, \quad V_{C3} = 0 \]

\[ V_o = V_{os} \]

Amplify mode (S1, S3, S5→off, S2, S4→on)

\[ V_{C1} = V_{os} - V_{I2} = \Delta V_{C1} = V_{I1} - V_{I2} \]
\[ V_{C2} = V_{os} - V_{I4} = \Delta V_{C2} = V_{I3} - V_{I4} \]
\[ \Delta Q_3 = \Delta Q_1 + \Delta Q_2 = C_1 \Delta V_{C1} + C_2 \Delta V_{C2} \]
\[ \Delta V_{C3} = \frac{\Delta Q_3}{C_3} = \frac{C_1}{C_3} (V_{I1} - V_{I2}) + \frac{C_2}{C_3} (V_{I3} - V_{I4}) \]
\[ V_o = \frac{C_1}{C_3} (V_{I1} - V_{I2}) + \frac{C_2}{C_3} (V_{I3} - V_{I4}) + V_{os} \]
Employing the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp.


Differential T/H Combined with Gain Stage

$\phi_1 \rightarrow \text{High}$
• Gain=$4C/C=4$
• Input voltage common-mode level removed $\Rightarrow$ opamp can have low input common-mode compliance
• Amplifier offset NOT removed