EECS 247 Lecture 18

ADC Converters
- Track & hold
  • T/H circuits
  • T/H combined with summing/difference function
  • T/H circuit incorporating gain & offset cancellation
  • T/H aperture uncertainty
- ADC architectures and design
  • Serial- slope type
  • Successive approximation
  • Flash ADC and its sources of error: comparator offset, sparkle code & meta-stability
- Comparator design
  • Single-stage open-loop amplifier
  • Cascade of open-loop amplifiers

Summary of Last Lecture

ADC Converters
- Sampling (continued)
  • Sampling switch considerations
    - Clock voltage boosters
  • Sampling switch charge injection & clock feedthrough
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching
- Track & hold
  • Flip around T/H
Flip-Around T/H-Basic Operation

$\phi_1 \to \text{high}$

$\phi_1$ and $\phi_2$ are control signals. $\phi_1$ is the clock signal, and $\phi_2$ is the hold signal.

$V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, $C$ is the capacitor, and $V_{CM}$ is the common-mode voltage.

1. **Charging $C$:**
   - $\phi_1$ is high, and $\phi_2$ is low.
   - S1 is closed, allowing $V_{IN}$ to charge $C$.
   - The opamp is in the non-inverting mode.
   - The charge is given by $Q_{\phi_1} = V_{IN} \times C$.
   - Note: Opamp must be stable in unity-gain configuration.

2. **Holding:**
   - $\phi_1$ is low, and $\phi_2$ is high.
   - S1 is open, and S2 and S3 are closed, holding the voltage.
   - $V_{OUT} = V_{IN}$.

Flip-Around T/H-Basic Operation

$\phi_2 \to \text{high}$

$\phi_1$ and $\phi_2$ are control signals. $\phi_1$ is the clock signal, and $\phi_2$ is the hold signal.

$V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, $C$ is the capacitor, and $V_{CM}$ is the common-mode voltage.

1. **Holding:**
   - $\phi_1$ is low, and $\phi_2$ is high.
   - S1 is open, and S2 and S3 are closed, holding the voltage.
   - $V_{OUT} = V_{IN}$.

2. **Charging $C$:**
   - $\phi_1$ is high, and $\phi_2$ is low.
   - S1 is closed, allowing $V_{IN}$ to charge $C$.
   - The opamp is in the non-inverting mode.
   - The charge is given by $Q_{\phi_2} = V_{OUT} \times C$.

Note: The opamp must be stable in unity-gain configuration.
Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit


- Gain = 1
- Issue: Large input common-mode compliance required
Differential Flip-Around T/H
Issues: Large Input Common-Mode Compliance

\[ V_{CM_{Vin}} = V_{out\_com} \cdot V_{sig\_com} \]

\[ \Delta V_{in\_cm} = V_{out\_com} - V_{sig\_com} \]

→ Drawback: Amplifier needs to have large input common-mode compliance

Input Common-Mode Cancellation

\[ V_{12} \]

\[ V_{11} \]

\[ V_{C1} \]

\[ V_{C2} \]

\[ V_{O1} \]

\[ V_{O2} \]

• Note: Shorting switch M3 added

Input Common-Mode Cancellation

- **Track mode** ($\phi$ high)
  - $V_{C1} = V_{I1}$
  - $V_{C2} = V_{I2}$
  - $V_{o1} = V_{o2} = 0$

- **Hold mode** ($\phi$ low)
  - $V_{o1} + V_{o2} = 0$
  - $V_{o1} - V_{o2} = -(V_{I1} - V_{I2})(C_1/(C_1 + C_3))$

→ Input common-mode level removed
* Will introduce active version in page 18

Switched-Capacitor Techniques Combining Track & Hold with Various other Functions

- T/H + Charge redistribution amplifier
- T/H & Input difference amplifier
- T/H & summing amplifier
- Differential T/H combined with gain stage
- Differential T/H including offset cancellation
T/H + Charge Redistribution Amplifier

### Track mode: \((S1, S3 \rightarrow \text{on} S2 \rightarrow \text{off})\)
- \(V_{C1} = V_{os} - V_{IN}\)
- \(V_C = 0\)
- \(V_o = V_{os}\)

### Hold Mode
- Offset NOT cancelled, but not amplified
- Input-referred offset = \((C_2/C_1) \times V_{OS}\), & often \(C_2 < C_1\)
- Can incorporate gain by having \(C_1 > C_2\)
T/H & Input Difference Amplifier

Sample mode:
(S1, S3 $\rightarrow$ on S2 $\rightarrow$ off)
$V_{C1} = V_{os} - V_{1I}$, $V_{C2} = 0$
$V_o = V_{os}$

T/H & Input Difference Amplifier

Cont'd

Subtract/Amplify mode (S1, S3 $\rightarrow$ off S2 $\rightarrow$ on)

During previous phase:
$V_{C1} = V_{os} - V_{1I}$, $V_{C2} = 0$
$V_o = V_{os}$

$V_{C1} = V_{os} - V_{I2}$
$\Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$

$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C1} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$

$V_o = \frac{C_1}{C_2}(V_{I1} - V_{I2}) + V_{os}$

$\rightarrow$ Offset NOT cancelled, but not amplified
$\rightarrow$ Input-referred offset = $(C_2/C_1)xV_{os}$, $C_2 < C_1$
Sample mode (S1, S3, S5 → on S2, S4 → off)

\[ V_{C1} = V_{os} - V_{I1}, \quad V_{C2} = V_{os} - V_{I3}, \quad V_{C3} = 0 \]

\[ V_o = V_{os} \]
T/H & Summing Amplifier Cont’d

Amplify mode (S1, S3, S5→off, S2, S4→on)

\[ V_{C1} = V_{IN} - V_{I2} = \Delta V_{C1} = V_{I1} - V_{I2} \]
\[ V_{C2} = V_{IN} - V_{I4} = \Delta V_{C2} = V_{I3} - V_{I4} \]
\[ \Delta Q_3 = \Delta Q_1 + \Delta Q_2 = C_{10}V_{C1} + C_{20}V_{C2} \]
\[ \Delta V_{C3} = \frac{\Delta Q_3}{C_3} = (\frac{C_1}{C_2})(V_{I1} - V_{I2}) + (\frac{C_2}{C_3})(V_{I3} - V_{I4}) \]
\[ V_O = \left( \frac{C_1}{C_2}(V_{I1} - V_{I2}) + \frac{C_2}{C_3}(V_{I3} - V_{I4}) + V_{IN} \right) \]

Differential T/H Combined with Gain Stage

Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp.

Differential T/H Combined with Gain Stage

$\phi_1 \rightarrow \text{High}$

- Gain $= 4C/C = 4$
- Input voltage common-mode level removed $\rightarrow$ opamp can have low input common-mode compliance
- Amplifier offset NOT removed

Differential T/H Including Offset Cancellation

- Operation during offset cancellation phase shown
- Auxiliary inputs added with $A_{main}/A_{aux} = 10$
- During offset cancellation phase:
  - Aux. amp configured in unity-gain mode: $\rightarrow$ offset stored on $C_{AZ}$ & canceled during the signal acquisition phase


Differential T/H Including Offset Cancellation

Operational Amplifier

- Operational amplifier $\rightarrow$ dual input folded-cascode opamp
- M3,4 auxiliary input, M1,2 main input
- To achieve 1/10 gain ratio $W_{M3,4} = 1/10 \times W_{M1,2}$ & current sources are scaled by 1/10
- M5,6,7 $\rightarrow$ common-mode control
- Output stage $\rightarrow$ dual cascode $\rightarrow$ high DC gain

$$V_{out} = g_{m1,2} o V_{in1} + g_{m3,4} o V_{in2}$$

**Differential T/H Including Offset Cancellation Phase**

- During offset cancellation phase AZ and S1 closed → main amplifier offset amplified by $\frac{g_{m1}}{g_{m2}}$ & stored on $C_{AZ}$
- Auxiliary amp chosen to have lower gain so that:
  - Aux. amp charge injection associated with opening of switch AZ → reduced by $\frac{A_{aux}}{A_{main}} = 1/10$
  - Insignificant increase in power dissipation resulting from addition of aux. inputs
- Requires an extra auto-zero clock phase

\[
(V_{INAZ+}-V_{INAZ-}) = -\frac{g_{m1,2}}{g_{m3,4}}V_{offset}
\]

**Track & Hold Aperture Time Error**

Transition from track to hold:
- Occurs when device turns fully off
  - $V_{CLK} = V_{in} + V_{TH}$
- Sharp fall-time wrt signal change
  - No aperture error
Track & Hold
Aperture Time Error

- Aperture error analysis applies to simple sampling network
- Bottom plate sampling → reduced aperture error
- Boosted clock → reduced aperture error

→ Clock edge fall/rise trade-off between switch charge injection versus aperture error

ADC Architecture & Design

ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - ...
- Oversampled ADCs
Various ADC Architectures
Resolution/Conversion Rate

- Oversampled & Serial
- Algorithmic e.g. Succ. Approx.
- Subranging e.g. Pipelined
- Folding & Interpolative
- Parallel & Time Interleaved

Resolution versus Signal Bandwidth

Ref: S. Chen, R. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-µm CMOS: IEEE J. of Solid-State Circuits, Vol. 41, No. 12, December 2006."
Serial ADC
Single Slope

- Counter starts counting @ $V_{Ramp}=0$
- Counter stops counting for $V_{IN}=V_{Ramp}$

$T_1$ is proportional to $V_{IN}$
Counter output proportional to $T_1=nT_{clock}$
Counter output proportional to $V_{IN}$
$2^N \times T_{clock} = V_{FS}$
Single Slope ADC

- Advantages:
  - Low complexity & simple
  - INL depends on ramp linearity & not component matching
  - Inherently monotonic

- Disadvantages:
  - Slow \( (2^N) \text{ clock pulses for N-bit conversion}) \text{(e.g. N=16)}
    \( f_{\text{clock}}=1\text{MHz} \rightarrow \text{needs 65000} \times 1\mu\text{s}=65\text{ms/conversion})\)
  - Hard to generate precise ramp required for high resolution ADCs
  - Need to calibrate ramp slope versus \( V_{IN} \)

- Better: Dual Slope, Multi-Slope

Serial ADC

Dual Slope

- First: \( V_{IN} \) is integrated for a fixed time \( (2^N \times T_{CLK}) \)
  \( \rightarrow V_o = 2^N \times T_{CLK} \times V_{IN} \) \( / \tau_{int} \)
- Next: \( V_o \) is de-integrated with \( V_{REF} \) until \( V_o = 0 \)
  \( \rightarrow \text{Counter output} = 2^N \times V_{IN} / V_{REF} \)
Dual Slope ADC

- Integrate $V_{in}$ for fixed time ($T_{INT}$), de-integrate with $V_{REF}$ applied $\Rightarrow T_{De-Int} \sim 2^N T_{CLK} V_{in}/V_{REF}$
- Most laboratory DVMs use this type of ADC

**Dual Slope ADC**

- **Advantage:**
  - Accuracy to 1st order independent of integrator time-constant and clock period
  - Comparator offset referred to input is attenuated by integrator high DC gain
  - Insensitive to most linear error sources
  - DNL is a function of clock jitter
  - Power line (60Hz) xtalk effect on reading can be canceled by: choosing conversion time multiple of 1/60Hz
  - High accuracy achievable (16+bit)

- **Disadvantage:**
  - Slow (maximum $2x2^N x T_{CLK}$ per conversion)
  - Integrator opamp offset results in ADC offset (can cancel)
  - Finite opamp gain gives rise to INL

http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - ...
- Oversampled ADCs

Successive Approximation ADC (SAR)

- Algorithmic type ADC
- Based on binary search over DAC output
Successive Approximation ADC

Example: 6-bit ADC & $V_{IN}=5/8V_{REF}$

- High accuracy achievable (16+ Bits)
- Need DAC to be accurate enough
- Require N clock cycles for N-bit conversion (much faster than slope type)
- Moderate speed (highest SAR conversion rate 2Ms/sec & 18 bits)

Example: SAR ADC

Charge Redistribution Type

- Built with binary weighted capacitors, switches, comparator & control logic
- T/H inherent in DAC
Charge Redistribution Type SAR DAC
Operation: Determining the MSB

- Operation starts by connecting all top plate to gnd and all bottom plates to \(V_{in}\).
- To test the MSB all top plate are opened bottom plate of 32C connected to \(V_{REF}\) & rest of bottom plates connected to ground → input to comparator= \(-V_{in} + V_{REF}/2\)
- Comparator is strobed to determine the polarity of input signal:
  - If negative MSB=1, else MSB=0
- The process continues until all bits are determined

Example: SAR ADC
Charge Redistribution Type

- To 1st order parasitic (\(C_p\)) insensitive since top plate driven from initial 0 to final 0 by the global negative feedback
- Linearity is a function of accuracy of C ratios
- Possible to add a C ratio calibration cycle (see Ref.)

ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - ...
- Oversampled ADCs

Flash ADC

- B-bit flash ADC:
  - DAC generates all possible $2^B - 1$ levels
  - $2^B - 1$ comparators compare $V_{IN}$ to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 1$
    - If $V_{DAC} > V_{IN} \rightarrow 0$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code
- Application example: 6-bit Flash ADC in Disk Drives with Gs/s conversion rate
**Flash Converter Characteristics**

- Very fast: only 1 clock cycle per conversion
  - \( \frac{1}{2} \) clock cycle \( \rightarrow \) \( V_{IN} \) & \( V_{DAC} \) comparison
  - \( \frac{1}{2} \) clock cycle \( \rightarrow 2^B - 1 \) to \( B \) encoding
- High complexity: \( 2^B - 1 \) comparators
- Input capacitance of \( 2^B - 1 \) comparators connected to the input node:
  - \( \rightarrow \) High capacitance @ input node
Flash ADC Converter Considerations

Assume simple comparator design

Depending on Vin level, lower comparators have M1 on & M2 off. Upper comparators have M1 off & M2 (m+n=2^k-1)

Total capacitance experienced by input source is a function of Vin

Also note Vin feedthrough to Vref taps via M1 & M2 G-S capacitance & Rs

When switches Mx open, charge injection and clock feedthru causes perturbation on R taps

Flash Converter Sources of Error

• Comparator input:
  – DC offset
  – Nonlinear input capacitance
  – Feedthrough of input signal to reference ladder
  – Kickback noise (disturbs reference)
  – Signal dependent sampling time (addition of T/H @ the input eliminates this problem)

• Comparator output:
  – Sparkle codes (… 0001011111)
  – Metastability
Flash ADC Converter
Example: 8-bit ADC Comparator Offset Considerations

- 8-bit → 255 comparators
- $V_{\text{REF}} = 1\, \text{V} \rightarrow 1\text{LSB} = 4\, \text{mV}$
- DNL < 1/2LSB → Comparator input referred offset < 2mV
- Assuming close to 100% yield, 2mV = 6$\sigma_{\text{offset}}$ → $\sigma_{\text{offset}} < 0.33\, \text{mV}$

\[
\text{Encoder}
\]
\[
\begin{array}{c}
\text{Digital} \\
\text{Output}
\end{array}
\]

Flash ADC Converter
Example: 8-bit ADC (continued)

→ $1\sigma_{\text{offset}} < 0.33\, \text{mV}$

- Let us assume in the technology used:
  - Offset-per-unit-$\sqrt{W \times L}$ = 3mV/$\mu$

\[
V_{\text{offset}} = \frac{3\, \text{mV}}{\sqrt{W \times L}} = 0.33\, \text{mV} \rightarrow W \times L = 83\, \mu^2
\]

Assuming: $C_{\text{ox}} = 9\, \mu F / \mu^2 \rightarrow C_{\text{gs}} = \frac{2}{3} C_{\text{ox}} W \times L = 496\, \mu F$

→ Total max. input capacitance: $255 \times 0.496 = 126.5\, \mu F$

- Issues:
  - Si area quite large
  - Large ADC input capacitance
  - Since depending on input voltage level different number of comparator input transistors would be on/off - total input capacitance varies as input varies
  - Nonlinear input capacitance could give rise to signal distortion

Flash ADC Converter
Example (continued)

Trade-offs:
- Allowing larger DNL e.g. 1LSB instead of 0.5LSB:
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduces the input capacitance by a factor of 4!
- Reducing the ADC resolution by 1-bit
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduce the input capacitance by a factor of 4

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Flash Converter
Maximum Tolerable Comparator Offset versus ADC Resolution

Assumption:
\( DNL = 0.5\text{LSB} \)

Note:
Graph shows max. tolerable offset, note that depending on min acceptable yield, the derived offset numbers are associated with 2\(\sigma\) to 6\(\sigma\) offset voltage.
**Typical Flash ADC Output Encoder**

- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM
- Ideally, for each code, only one ROM row is on

**Sparkle Codes**

- Erroneous 0 (comparator offset?)
- Correct Output: 1000
- Problem: Two rows are on
- Erroneous Output: 1110
- → Up to ~ ½ FS error!!
Sparkle Tolerant Encoder

- Protects against a single sparkle.
- Possible to improve level of sparkle protection by increasing # of NAND gate inputs

Ref: C. Mangelsdorf et al, “A 400-MHz Flash Converter with Error Correction,” JSSC February 1990, pp. 997-1002

Meta-Stability

Different gates interpret metastable output X differently

Correct output: 1000
Erroneous output: 0000

Solutions:
- Add latches to comparator outputs (high power)
- Gray encoding

Gray Encoding

Example: 3bit ADC

<table>
<thead>
<tr>
<th>Thermometer Code</th>
<th>Gray</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_7 T_6 T_5 T_4 T_3 T_2 T_1</td>
<td>G_3 G_2 G_1</td>
<td>B_3 B_2 B_1</td>
</tr>
<tr>
<td>0 0 0 0 0 0 0 0</td>
<td>0 0 0</td>
<td>0 0 0</td>
</tr>
<tr>
<td>0 0 0 0 0 1 0 0</td>
<td>0 0 1</td>
<td>0 0 1</td>
</tr>
<tr>
<td>0 0 0 1 1 1 1 1</td>
<td>0 1 0</td>
<td>0 1 0</td>
</tr>
<tr>
<td>0 1 1 1 1 1 1 1</td>
<td>1 1 0</td>
<td>1 1 0</td>
</tr>
<tr>
<td>1 1 1 1 1 1 1 1</td>
<td>1 0 0</td>
<td>1 1 0</td>
</tr>
</tbody>
</table>

- Each T_i affects only one G_i
- Metastability in one T output affects only one of the G bits (unlike binary)
- Protects also against sparkles
- Follow Gray encoder by (latch and) Gray-to-binary encoder

\[ G_1 = T_1 \overline{T_3} + T_5 \overline{T_7} \]
\[ G_2 = T_2 \overline{T_6} \]
\[ G_3 = T_4 \]

Voltage Comparators

Play an important role in majority of ADCs
Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

If \( V_{i+} - V_{i-} > 0 \) \( \rightarrow \) \( V_{out} = "1" \)
If \( V_{i+} - V_{i-} < 0 \) \( \rightarrow \) \( V_{out} = "0" \)
Voltage Comparator Architectures

Comparator architecture choices:

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing has to be compatible with driving digital logic circuits
  - Open-loop amplification → no frequency compensation required
  - Precise or linear transfer function not required

- Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation:
    • Latch-only comparator
    • Low-gain preamplifier + high-sensitivity latch

- Sampled-data comparators
  - T/H input
  - Offset cancellation

Comparator Built with High-Gain Amplifier

Amplify $V_{\text{in}}(\text{min})$ to $V_{\text{DD}}$
$\rightarrow V_{\text{in}}(\text{min})$ determined by ADC resolution

Example: 12-bit ADC with:
- $V_{\text{FS}} = 1.5V \rightarrow 1\text{LSB} = 0.36\text{mV}$
- $V_{\text{DD}} = 1.8V$

$\rightarrow$ For 1.8V output & 0.5LSB resolution:

$$A_{\text{Mo}} = \frac{1.8V}{0.18\text{mV}} \approx 10,000$$
Comparator Design

1- Single-Stage Amplification

- Amplifier maximum Gain-Bandwidth product \( f_u \) for a given technology, typically a function of maximum device \( f_t \)

\[ f_u = \text{unity-gain frequency, } f_e = \text{-3dB frequency} \]

\[ f_u = \frac{f_u}{A_v} \]

**Example:** \( f_u = 10^{10} \text{GHz} \) & \( A_v = 10,000 \)

\[ f_u = \frac{10^{10}}{10,000} \approx 1 \text{MHz} \]

\[ \tau_{\text{settling}} = \frac{1}{2\pi f_u} \approx 0.16 \mu s \]

Allow a few \( \tau \) for output to settle

\[ f_{\text{Max}} = \frac{1}{5\tau_{\text{settling}}} \approx 1.26 \text{MHz} \]

Too slow for majority of applications!

→ Try cascade of lower gain stages to broaden frequency of operation

**Assumption:** Single pole amplifier

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Comparator Design

2- Cascade of Open Loop Amplifiers

The stages identical → small-signal model for the cascades:

- One stage:

\[ |A_v(0)| = g_m R_L \]

\[ \omega_0 = -3 \text{dB frequency} = \frac{1}{R_L C_T} \]

\[ \omega_u = -\text{unity gain frequency} = G \times \text{BW} = \frac{g_m}{C_T} \]

\[ \omega_b = \frac{\omega_u}{|A_v(0)|} \]
Open Loop Cascade of Amplifiers

For an N-stage cascade:

\[ A_T(j\omega) = \left( A_T(0) \right) \frac{N}{1 + \frac{\omega}{\omega_{0N}}} \]

Define

\[ \omega_{0N} = -3\text{dB frequency of the N-stage cascade} \]

Then

\[ |A_T(j\omega_{0N})| = \frac{|A_T(0)|^N}{\sqrt{2}} \]

and

\[ \omega_{0N} = \frac{\omega_N}{\sqrt{2^{N-1}}} = \frac{\omega_N}{|A_T(0)|\sqrt{2^{N-1}}} \]

Example: N=4, A_T=10000 \[\Rightarrow\] \omega_{0N}=430\omega_N

Open Loop Cascade of Amplifiers

For \(|A_T(\text{DC})|=10,000\)

| N | \(\omega_{0N}/\omega_N\) | \(|A_T(0)|\) |
|---|---|---|
| 1 | 1 | 10,000 |
| 2 | 64 | 100 |
| 3 | 236 | 21.5 |
| 4 | 435 | 10 |
| 5 | 611 | 6.3 |
| 10 | 1067 | 2.5 |
| 20 | 1185 | 1.6 |

Example:

\(N=3, f_d=10\text{GHz} \quad \& \quad |A_T(0)|=10000\)

\[ f_{ON} = \frac{10\text{GHz}}{(10,000)^{1/3}} \approx 237\text{MHz} \]

\[ \tau_{\text{setting}} = \frac{1}{2\pi f_o} = 0.7\text{ns} \]

Allow a few \(\tau\) for output to settle

\[ f_{\text{Clock}} \rightarrow \frac{1}{5\tau_{\text{setting}}} \approx 290\text{MHz} \]

\(f_{\text{max}}\) improved from 1.26MHz to 290MHz \[\Rightarrow\] X236
Open Loop Cascade of Amplifiers

Offset Voltage

- From offset point of view: high gain/stage is preferred
- Choice of # of stage \( \rightarrow \) bandwidth vs offset tradeoff

\[
A_T = A_1 \cdot A_2 \cdot A_3
\]

Input-referred offset \( \rightarrow V_{os} = \frac{V_{os1} + V_{os2} + V_{os3}}{A_1 \cdot A_2} \)

---

Open Loop Cascade of Amplifiers

Step Response

- Assuming linear behavior (not slew limited)

\[
\begin{align*}
V_{o1} &= \frac{1}{C_1} \int_0^t g_m v_{in} dt = \frac{g_m v_{in}}{C} t \\
V_{o2} &= \frac{1}{C_2} \int_0^t g_m V_{o1} dt = \frac{g_m}{2C} t V_{in}^2 \\
V_{o3} &= \frac{1}{C_3} \int_0^t g_m V_{o2} dt = \frac{g_m}{3C} t^3 V_{in}^3 \\
\end{align*}
\]
Open Loop Cascade of Amplifiers
Step Response

• Assuming linear behavior

\[ \frac{C}{g_m} \] \[ N + 1 \text{ stages} \]

\[ V_{out} = \left( \frac{g_m}{C} \right)^N \left( \frac{t}{N} \right) V_{in} \]

For the output to reach a specified \( V_{out} \) (i.e., \( V_{out} = V_{in} \)) the delay is

\[ \tau_D = \left( \frac{C}{g_m} \right)^{\left( \frac{t}{V_{out}/V_{in}} \right)} \]