[Final] Past Exams - 2019 and older #1310

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Peyrin Kao STAFF
2 months ago in Exam – Final

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VIEWS

You can find the past exams here: https://cs61c.org/su22/resources/exams/

When posting questions, please reference the semester, exam, and question in this format so it's easier for students and staff to search for similar questions:

Semester-Exam-Question Number

For example: **SP19-Final-Q1**, or **SU19-MT2-Q3**

Spring 2019 final walkthrough

Summer 2019 final walkthrough

- Q1 Potpourri: https://youtu.be/FY5dAMrXvxo
- Q2 FSM: https://youtu.be/gmHbw6LSeSw
- Q3 C Coding: https://youtu.be/v4B1WTs5UNU
- Q4 RISC-V: https://youtu.be/2VHjG-gy9Dk
- Q5 Data-Level Parallelism: https://youtu.be/oG9Rrzmi0M4
- Q6 RAID and ECC: https://youtu.be/rfCNTIzNZ2M
- Q7 Caches: https://youtu.be/xojc8YZaO3Q
- Q8 Spark: https://youtu.be/A37BFXRXmm0
- Q9 Datapath: https://youtu.be/q-T4N3hBhUM
- Q10 Digital Logic: https://youtu.be/3RI36lsDSg4
- Q11 Virtual Memory: https://youtu.be/5_2fKsK4I34

Added 2022/08/10:

Extremely rough draft SP19 final solutions

Anonymous Deer 2mth #1310af ✓ Resolved

Are parts 1-7 of Q1 (Sp19 final) out of scope?

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Caroline Liu STAFF 2mth #1310ba

Part 7 isn't out of scope since it's considered to be speedup (part of parallelism, Amdahl's

Law in a way) but 1-6 is since PUE (power usage effectiveness) and I/O weren't covered this semester!

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Anonymous Jay 2mth #1310ad ✓ Resolved

SP-19-Final-8.4 https://cs61c.org/su22/pdfs/exams/draft-sp19-final-solutions.pdf

> In the first iteration of the loop, we bring in the first block of arr (index 0). Also, we have to bring in the first block of C (index 0). If the cache were direct-mapped, the C block would kick out the arr block, even though we haven't used all the elements of the arr block yet.
why could block of C kick out block of arr? same memory?

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P Peyrin Kao STAFF 2mth #1310ae

Same index.

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Anonymous Jay 2mth #1310f ✓ Resolved

SP-19-Final-Q3.4 Page 12: https://cs61c.org/su22/pdfs/exams/draft-sp19-final-solutions.pdf

> More comprehensive answer: As mentioned in the previous subpart, array A takes up
> 8 pages of memory. This means that A has 8 VPNs that we need to translate to 8 PPNs. This means that we need 8 PTEs to map each of the 8 VPNs to 8 PPNs. The same logic applies to B, so we need 16 PTEs in total.

How do we convert from memory to PTEs?

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P Peyrin Kao STAFF 2mth #1310aa

Memory can be divided into pages (i like to think of pages as a unit of measurement). Then given how many pages you need, you need one PTE for each page of data memory.

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Anonymous Jay 2mth #1310e ✓ Resolved

SP-19-Final-Q2.5 page 9 here https://cs61c.org/su22/pdfs/exams/draft-sp19-final-solutions.pdf

> The longest path in the EX stage starts at the pipeline registers, passes through Box II (or Box III) and the ALU, and ends at the next pipeline registers. This has a combinatorial delay of 75 + 200 = 275 ps.

Where we get the 75 from? Both box II and box III should have 25 ps, plus register setup, we get 75 = 25 + 25 + 20, is that the way to do it?

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P Peyrin Kao STAFF 2mth #1310ab

The question says to assume the delay of the box is 75 ps, I think?

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Anonymous Moose 2mth #1310d ✓ Resolved

(Referring to summer 2018 q6 pt 3, but also just general concept question), do write misses on a no write allocate cache not count as misses/factor in to the hit rate? If so, why not? That's what the solution seems to imply.

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P Peyrin Kao STAFF 2mth #1310ac

I think write misses still count as misses in general, unless otherwise stated.

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Anonymous Okapi 2mth #1310a ✓ Resolved

Do we have to know how to program using RISC-V and atomics? It was talked about once in lecture and it was one slide long. Only anoswap was briefly covered.

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B Bolong Zheng 2mth #1310b

are atomics out of scope?

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P Peyrin Kao STAFF 2mth #1310c

The SP19 final atomics question is out of scope.

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