[Final] Past Exams - 2022 #1313

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2 months ago in Exam – Final

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VIEWS

You can find the past exams here: https://cs61c.org/su22/resources/exams/

When posting questions, please reference the semester, exam, and question in this format so it's easier for students and staff to search for similar questions:

Semester-Exam-Question Number

For example: **SP22-Final-Q1**, or **SP22-MT2-Q3**

Anonymous Leopard 2mth #1313dd ✓ Resolved

SP22-Final-Q3.7

Can someone please explain why they won't yield the expected behavior? I'm confused about this.

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Peyrin Kao STAFF 2mth #1313de

See the midterm.

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Anonymous Camel 2mth #1313ce ✓ Resolved

SP22-Final-Q7.1

Why wouldn't you divide page table size by PTE in order to get the number of entries, and then take the log_2 of it to get 9?

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Anonymous Camel 2mth #1313cf

Also for this sort of question if we get the first one wrong, and the other answers depend on it will we get all of them wrong?

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Peyrin Kao STAFF 2mth #1313da

it's not guaranteed that the page table fits on one page.

We gave partial credit to avoid double-jeopardy on this question, if I remember correctly.

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Anonymous Camel 2mth #1313cd ✓ Resolved

SP22-Final-Q6.5

What causes the data race here, I don't fully understand the explanation, is it saying it's caused by the chance that index 6 (or other composite numbers) could be written to by multiple threads, specifically the index's divisors, in this case 6, 3, or 2?

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P Peyrin Kao STAFF 2mth #1313db

in serial access, if you set `primes[j] = 1`, you'll never access `primes[j]` again because of the if-check.

In parallel access, multiple threads might access `primes[j]` at the same time.

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Anonymous Parrot 2mth #1313be ✓ Resolved

In question 6.3, why we have capacity miss instead of conflict miss. Say we have first 1/4 of the array in the cache. Since it's dirrect mapped cache, we have 0x00000000 in our cache, and when we access the next 1/4 of the array which starts at index 4096, we have 0x00001000 since 4096 is 2^12, the 1 should appear in the 13th bit. And we know offset and index have 12 bits, so this address has the same index and offset but different tag with 0x00000000, so 0x0000000 and it's cache line will be evicted. I thought this situation we will consider it's a conflict miss. Could some one explain to me why?

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P Peyrin Kao STAFF 2mth #1313bf

The cache is full when something gets evicted, so it's a capacity miss.

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Anonymous Parrot 2mth #1313ca

Even it's also a conflict miss, we count it as capacity miss?

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P Peyrin Kao STAFF 2mth #1313cb

Replying to Anonymous Parrot

I think of capacity as taking "precedence" over conflict. If the cache is full, it's capacity, even if it happens to map to an existing index (which it always will).

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Anonymous Parrot 2mth #1313cc

Replying to Peyrin Kao

Oh, ok thanks a lot.

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J James Tang 2mth #1313dc

Replying to Peyrin Kao

Do capacity misses take precedence over compulsory misses?

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P Peyrin Kao STAFF 2mth #1313df

Replying to James Tang

No, compulsory misses take precedence.

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Anonymous Clam 2mth #1313ae ✓ Resolved

SP22-Final-Q6.3

Why does primes[4] brings in primes[0] to primes[127] instead of primes[4] to primes[131] ?

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Anonymous Anteater 2mth #1313af ENDORSED

Although I havent looked up the question. I'm assuming it has to do with the way caching works. Say I have a T/I/O breakdown of 4/4/4

If I try to access address 0xF1E

I will have Tag = 0b1111

Index = 0b0001

Offset = 0b1110

Yet I will pull the block of memory representing 0xF10 to 0xF1F into the cache. We get out blocks on a block alignment. So basically we ignore the offset

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Anonymous Clam 2mth #1313ba

Thanks for the explanation!

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Anonymous Kudu 2mth #1313ad ✓ Resolved

SP22-Final-Q3.10

Can anyone explain the coherence miss of A? Is this question in scope? and why "Due to repeated data invalidations, memory accesses in A will tend to be around the same as L3 cache access times or longer".

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P Peyrin Kao STAFF 2mth #1313bb

Yes, false sharing is in scope. Even though each thread is accessing different elements, they're all trying to write to the same cache block, which causes cache coherency issues.

...

A Adam Ousherovitch 2mth #1313bd

So, in what cases would you actually want to use parallelism if you do it at the cost of coherency issues.

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Anonymous Kudu 2mth #1313ac ✓ Resolved

SP22-Final-Q5.3

For this question, what does "a new instruction format" mean?

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P Peyrin Kao STAFF 2mth #1313bc

We have R-type, I-type, B-type, etc. This option is asking if you need to add another instruction type.

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Anonymous Meerkat 2mth #1313f ✓ Resolved

should SP22-Final-Q7.2 say "so we need 26 bits to address every byte of physical memory." rather than 16?

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P Peyrin Kao STAFF 2mth #1313aa

Please tag the question properly in your post!

Yes, that's a typo. I'll fix.

...

Anonymous Hawk 2mth #1313c ✓ Resolved

SP22-Final-Q2

Why don't we need to consider the time for short-answer? I am a little confused.

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P Peyrin Kao STAFF 2mth #1313d

You have everybody on earth to help grade, so while some TAs are grading long-answer questions, you could have other TAs grade the short-answer questions at the same time.

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Anonymous Hawk 2mth #1313e

so as long as the short-answer time is smaller than long-answer, we do not have to care about short-answer time when we are given infinite TA?

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P Peyrin Kao STAFF 2mth #1313ab

Replying to Anonymous Hawk

It depends on the constraints of the question. In this question, we said that each TA can grade a question separately, so if we have billions of TAs, we just give a different question to each TA. Then the time it takes to finish is limited by the TAs grading one long-answer question.

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Anonymous Toad 2mth #1313a ✓ Resolved

SP22-Final-Q1.5 and Q3.7

Are these questions in scope?

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P Peyrin Kao STAFF 2mth #1313b

DMA is not in scope. `#define` statements are in scope I believe.

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