EECS 16A Designing Information Devices and Systems I
Spring 2017 Babak Ayazifar, Vladimir Stojanovic Homework 8

This homework is due Saturday, March 18, 2017, at 23:59.
Self-grades are due Thursday, March 23, 2017, at 23:59.

Submission Format
Your homework submission should consist of **one** file.

- `hw8.pdf`: A single pdf file that contains all your answers (any handwritten answers should be scanned). If you used an IPython notebook, it should also be saved as a pdf.

  If you do not attach a pdf of your IPython notebook, you will not receive credit for problems that involve coding. Make sure your results and plots are showing.

Submit this file to the appropriate assignment in Gradescope.

1. (PRACTICE) Super-Capacitors

In order to enable small devices for the "Internet of Things" (IoT), many companies and researchers are currently exploring alternative means of storing and delivering electrical power to the electronics within these devices. One example of these are "super-capacitors" - the devices generally behave just like a "normal" capacitor, but have been engineered to have extremely high values of capacitance relative to other devices that fit in to the same physical volume.

Your startup named **IoT4eva** is designing a new device that will revolutionize the process of making pizza, and you've been put in charge of selecting an energy source for it. You can't find a battery that quite suits your needs, so you decide to try out some super capacitors in various configurations. The super capacitors will be charged up to a certain voltage in the factory, and will then act as the power supply (source of voltage) for the electronics in your device.

(a) Assuming that the electronics in your device can be modeled as drawing a constant current with a value of I_{load}, draw circuit models for your device using the following configurations of super-capacitors as the power supply for the electronics:

  i. a single super-capacitor
  ii. two super-capacitors stacked in series
  iii. two super-capacitors connected in parallel

(b) If each super-capacitor is charged to an initial voltage V_{init} and has a capacitance of C_{sc}, for each of the three configurations above, write an expression for the voltage supplied to your electronics as a function of time after the device has been activated (t).

(c) Now let's assume that your electronics require some minimum voltage V_{min} in order to function properly. For each of the three super-capacitor configurations, write an expression you could use to calculate the lifetime of the device.

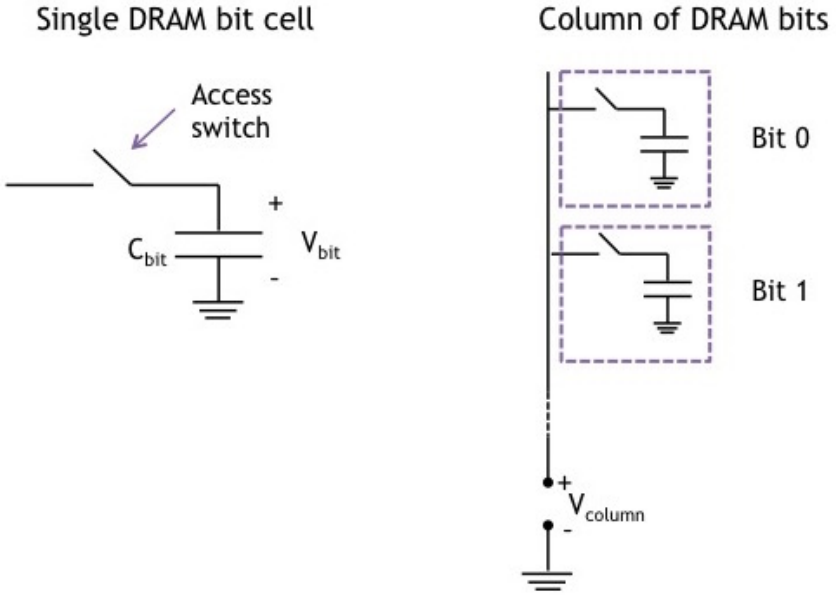
(d) Assuming that a single super-capacitor doesn't provide you sufficient lifetime and so you have to spend the extra money (and device volume) for another super-capacitor. Which configuration would you pick and why would you pick one over the other?

- Config 2: two super-capacitors stacked in series
- Config 3: two super-capacitors connected in parallel

2. Dynamic Random Access Memory (DRAM)

Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor are typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store > 8 billion bits and is sold for $\sim \$3-5$.

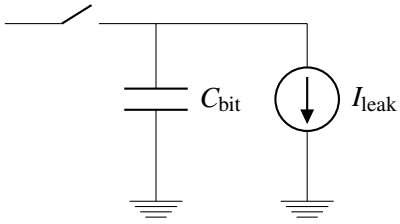
At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location. As also shown below, in order to pack as many bits together as possible on to a single chip, rather than running a massive number of wires to access every single bit of the DRAM individually, the bits are arranged in to a set of columns, where each column uses a single wire to access information from one of the bits; By turning on the access switch within the particular bit cell via the single column wire, the corresponding bit is accessed (while leaving all of the switches in the rest of the cells off).



Building even on only what we've learned about capacitors so far, because of the underlying simplicity of this structure we can understand a lot about how DRAMs work and are designed. Thus, in this problem we

will examine some of the issues and tradeoffs that actual DRAM designers deal with when engineering their products.

(a) In any real capacitor, there is always a path for charge to "leak" off of the capacitor and cause it to eventually discharge. In DRAMs the dominant path for this leakage to happen is through the access switch, but let's ignore this for now and assume that this leakage can be modeled as shown below:



This leakage is actually responsible for the "D" in "DRAM" - the memory is "dynamic" because after a cell is written by storing some charge on to its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 18fF$ (note that $1fF = 10^{-15}F$) and the capacitor is initially charged to 1.2V to store a "1". V_{bit} must be > 0.8V in order for the circuits outside of the column to properly read out the bit stored in the cell as "1". What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for > 1ms?

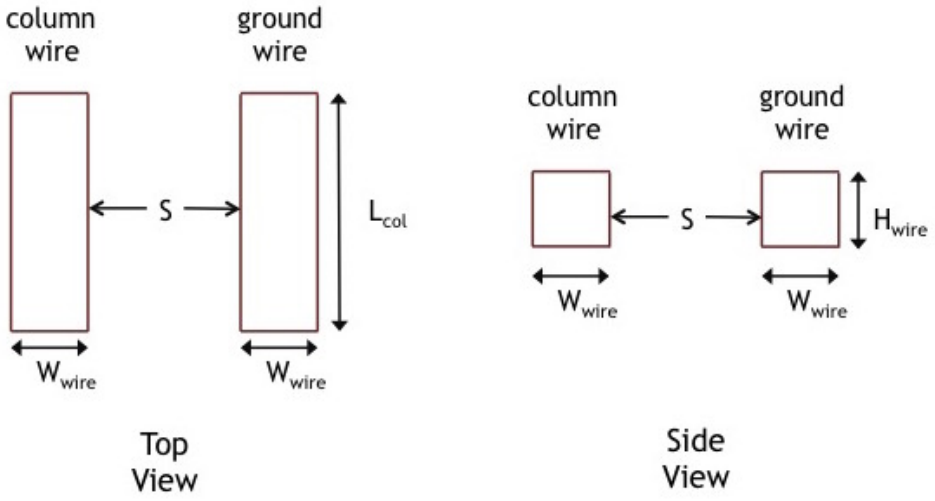
(b) One of the key decisions a DRAM designer has to make is how many cells to include on a single column. Packing more cells on a single column reduces the total number of wires in the chip, saving some chip space and hence cost (chip cost is strongly related to the physical size of the chip), but as we will see next, making the column too long may stop the DRAM from working properly.

Every time we add another DRAM cell on to the column, the wire that connects all of these cells together must get longer. As shown below, the column wire runs next to another wire that is connected to ground (the same ground that is connected to one side of the capacitors in the DRAM cells). This means that the column wire will have some capacitance to ground.

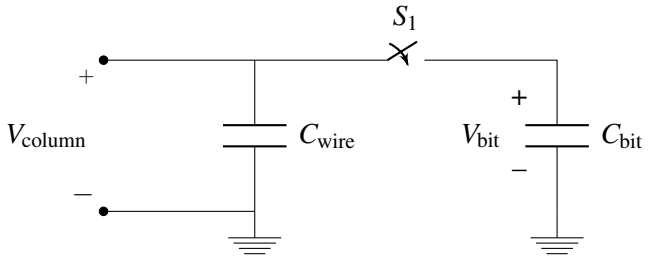
Let's assume that each DRAM cell that gets added also adds an additional length 0.5μm (i.e., 0.5×10^{-6} m) to the column and ground wires. The spacing between the column and ground wires $S = 0.1\mu$m and the height of the wire $H_{\text{wire}} = 0.5\mu$m. If we put 1024 DRAM cells on each column, what is the capacitance between the column wire and the ground wire? Note that you can assume that the two wires are separated by air but in a real chip they would be separated by silicon dioxide, but we'll ignore that for this exercise. You should also assume that all of the capacitance is purely parallel plate. Recall that the capacitance of a two parallel plates separated by air is $C = \frac{\varepsilon A}{d}$, where A is the area of the plate, d is the perpendicular distance between the two plates, and $\varepsilon = 8.854 \cdot 10^{-12} \frac{\text{F}}{\text{m}}$ is the permittivity of air.

(c) In order to read out the value of an individual cell, we turn on the access switch within that cell to connect the capacitor to the column wire, and then read out the resulting voltage on the column wire relative to ground. Note that before this readout operation occurs, the column wire is connected to ground to make sure that its capacitance is discharged, i.e. there is no charge on the wire before it is connected to the capacitor.

The situation described above can be modeled using the circuit shown below; note that for simplicity we will ignore the leakage current and its effects from here on out. If $C_{\text{bit}} = 18fF$, $C_{\text{wire}} = 20fF$ (note



this may or may not be your answer to part b), and the DRAM cell has a 0 stored in it (i.e., V_{bit} is set to 0V before S_1 is turned on), what is V_{column} after switch S_1 is turned on (i.e., makes a connection between the capacitor and column wire)? What will V_{column} be in the case that the DRAM cell has a 1 stored in it, meaning the V_{bit} is set to 1.2V before S_1 is turned on?



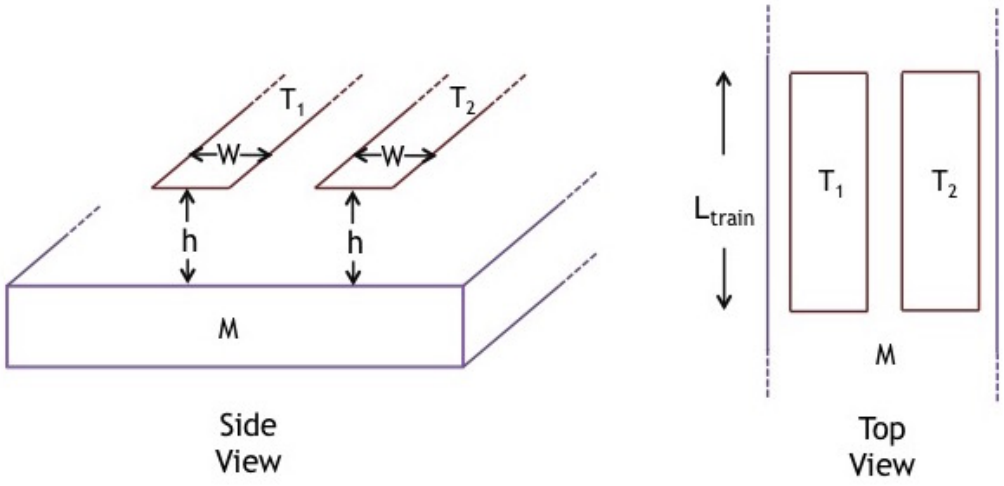
(d) The minimum voltage the readout circuit needs to reliably detect a "1" in a DRAM cell is 0.4V. Considering $C_{\text{bit}} = 18fF$, and using the same dimensions provided in part b) for the wires, what is the maximum number of cells that can be stacked together on to a single DRAM column while still meeting this minimum voltage requirement for the readout?

Note: Real DRAMs do things slightly differently in terms of the voltage they initially set the column wire to but use the same basic concept as described above.

3. Mag-lev Train Height Control System

One of the fastest forms of land transportation are trains that actually travel slightly elevated from ground using magnetic levitation (or "mag-lev" for short). Ensuring that the train stays at a relatively constant height above its "tracks" (the tracks in this case are what provide the force to levitate the train and propel it forward) is critical to both the safety and fuel efficiency of the train. In this problem we'll explore how we can use ideas very similar to the capacitive touchscreen we learned about in class (and in the lab) to realize such a height control system. (Note that real mag lev trains may use completely different and much more sophisticated techniques to perform this function, so if you e.g. get a contract to build such a train you'll probably want to do more research on the subject.)

(a) As shown below, let's imagine that all along the bottom of the train, we put two parallel strips of metal (T_1, T_2), and that on the ground below the train (perhaps as part of the track) we have one solid piece of metal (M).



Assuming that the entire train is at a uniform height above the track and ignoring any fringing fields (i.e., all capacitors are purely parallel plate), as a function of L_{train} (the length of the train), W (the width of T_1/T_2), and h (the height of the train off of the track), what is the capacitance between T_1 and M? How about the capacitance between T_2 and M?

(b) Any circuit on the train can only make direct contact at T_1 and T_2. To detect the height of the train, it would only be able to measure the effective capacitance between T_1 and T_2. Draw a circuit model showing how the capacitors between T_1 and M and between T_2 and M are connected to each other.

(c) Using the same parameters as in part (a), provide an expression for the capacitance between T_1 and T_2.

(d) Let's assume that instead of just detecting the height (by measuring the capacitance between T_1 and T_2), we also want to control it. Let's assume that the device we use to control the height takes in only one of only two commands: increase the height, or decrease the height. In particular, this device is controlled by an input voltage. If that voltage is greater than 2.5 V it will push the train higher above the track, and if it is less than 2.5 V it will let the train move down closer to the track.

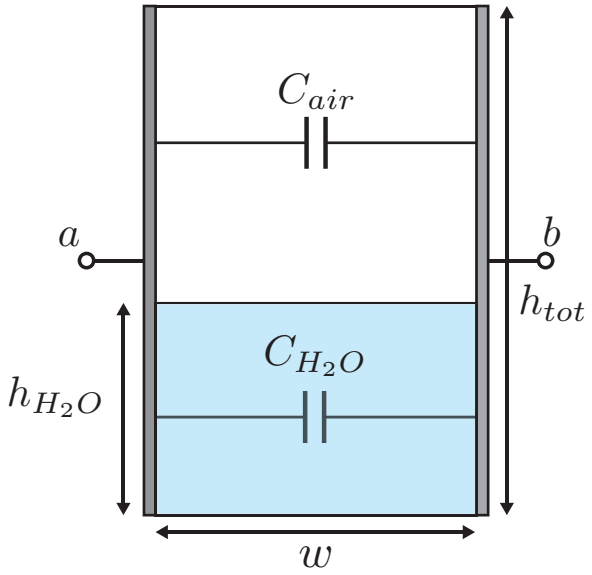
Assuming that the train is 100m long ($L_{\text{train}} = 100\text{m}$) and that the T_1/T_2 metals are each 1cm wide ($W = 1\text{cm}$), design a circuit that will drive the control device to make the train levitate 1cm above the track. Be sure to show how your circuit is connected to T_1 and T_2, and be as specific as possible in terms of the component values you would use. You can use any combination of switches, voltage sources, current sources, resistors, and capacitors that you would like to implement this circuit.

(e) So far we've assumed that the height of the train off of the track is uniform along its entire length, but in practice this may not be the case. Suggest and sketch a modification to the basic sensor design (i.e., the two strips of metal T_1/T_2 along the entire bottom of the train) that would allow you to measure the height at the train at 4 different locations.

4. It's finally raining!

A lettuce farmer in the Salinas valley has grown tired of weather.com's imprecise rain measurements. So, she decided to take matters into her own hands by building a rain sensor. She placed a rectangular tank outside

and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.

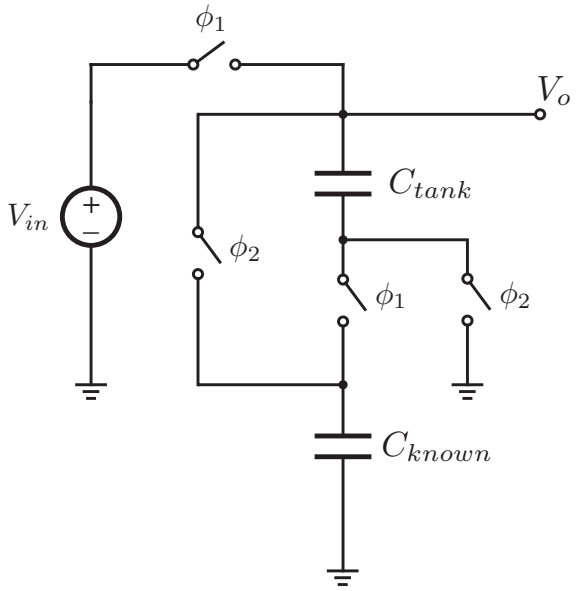


The width and length of the tank are both w (i.e. the base is square) and the height of the tank is h_{tot}.

(a) What is the capacitance between terminals a and b when the tank is full? What about when it is empty? Note: the permittivity of air is ε, and the permittivity of rainwater is 81ε.

(b) Suppose the height of the water in the tank is h_{H_2O}. Modeling the tank as a pair of capacitors in parallel, find the total capacitance between the two plates. Call this capacitance C_{tank}.

(c) After building this capacitor, the farmer consults the Internet to assist her with a capacitance measuring circuit. A random Anon recommends the following:



In this circuit, C_{tank} is the total tank capacitance that you calculated earlier. C_{known} is some fixed and known capacitor. Find the voltage V_o in phase ϕ_2 as a function of the height of the water. Note that

in phase ϕ_1 all switches labeled ϕ_1 are closed and all switches labeled ϕ_2 are open. In phase ϕ_2, all switches labeled ϕ_1 are open and all switches labeled ϕ_2 are closed. You should also assume that before any measurements are taken, the voltages across both C_{known} and C_{tank} are initialized to $0V$.

(d) Use IPython (or any other tool or just do it by hand) to plot this voltage V_o as a function of the height of the water. Vary the tank from empty to full. Use values of $V_{\text{in}} = 12\text{V}$, $w = 0.5\text{m}$, $h_{\text{tot}} = 1\text{m}$, and $\varepsilon = 8.854 \times 10^{-12}\text{F/m}$. This ε is called the *permittivity of free space*. For C_{known} use a similar tank that is known to always be empty.

(e) With the previous part, we were able to derive an expression for V_o. What does V_o represent? It's something we can measure! Our original goal was to determine what the height of the water in the tank without having to look inside it. Rewrite the last part to solve for h_{water}.

(f) How about we perform a sanity check on our answer. What are the units of your result for V_o and for h_{water}?

5. Homework process and study group

Who else did you work with on this homework? List names and student ID's. (In case of hw party, you can also just describe the group.) How did you work on this homework?
Working in groups of 3-5 will earn credit for your participation grade.