RC Circuits / Differential Equations

OUTLINE

- Review: CMOS logic circuits & voltage signal propagation
- Model: *RC* circuit → differential equation for $V_{out}(t)$
- Derivation of solution for $V_{out}(t)$ → propagation delay formula

EE16B, Fall 2015

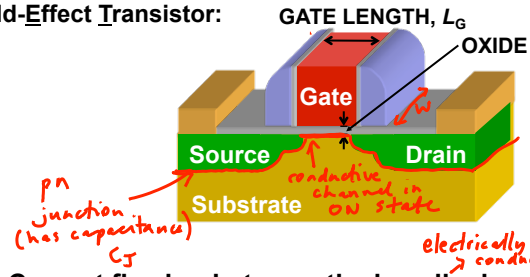
Meet the Guest Lecturer

Prof. Tsu-Jae King Liu

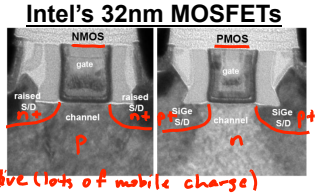
- Joined UCB EECS faculty in 1996
- Courses taught: 40, 105, 130, 143, 290D, 375
- Research in nanoelectronic & nanomechanical devices

The MOSFET

Metal-Oxide-Semiconductor Field-Effect Transistor:



Intel's 32nm MOSFETs

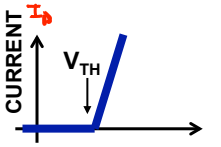


- Current flowing between the heavily doped SOURCE & DRAIN regions is controlled by the voltage on the GATE electrode
- N-channel & P-channel MOSFETs operate in a complementary manner

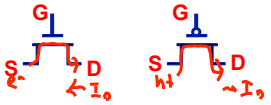
negatively charged electrons (e^-) — positively charged "holes" (h^+)

↳ "CMOS"

ON: $V_G > V_S + V_{TH}$ $\quad V_G < V_S - V_{TH}$

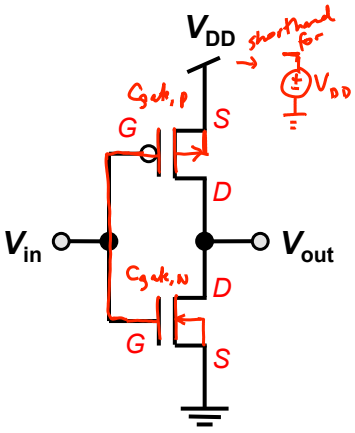


CIRCUIT SYMBOLS:



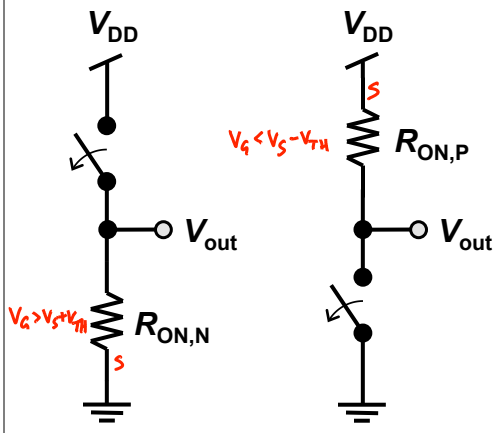
The CMOS Inverter

CIRCUIT



✓ Low static power consumption, since one transistor is always off in steady state

SWITCH MODELS

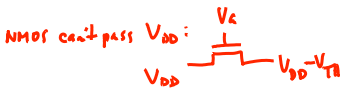


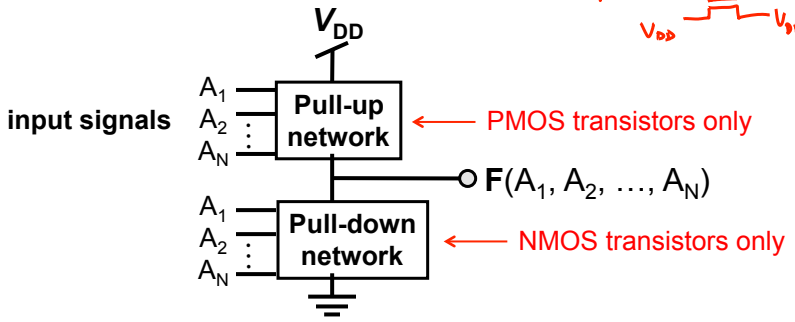
$V_{IN} = V_{DD}$ $\qquad$ $V_{IN} = 0$ V

$V_{DD} > V_{TH}$

Pull-Down and Pull-Up Devices

- In CMOS logic gates, NMOS transistors are used to connect the output to **GND**, whereas PMOS transistors are used to connect the output to V_{DD}.
  - An NMOS transistor functions as a ***pull-down device*** when it is turned on (gate voltage = V_{DD})
  - A PMOS transistor functions as a ***pull-up device*** when it is turned on (gate voltage = **GND**)





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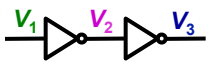
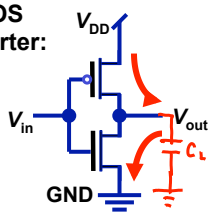
Voltage Signal Propagation

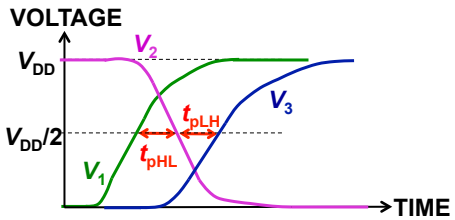
- When an input voltage of a logic gate is changed, there is a ***propagation delay*** before the output of the logic gate changes, due to capacitive loading at the output.

CMOS inverter chain



CMOS inverter:





Propagation delay is measured between the 50% transition points of the input and output signals.

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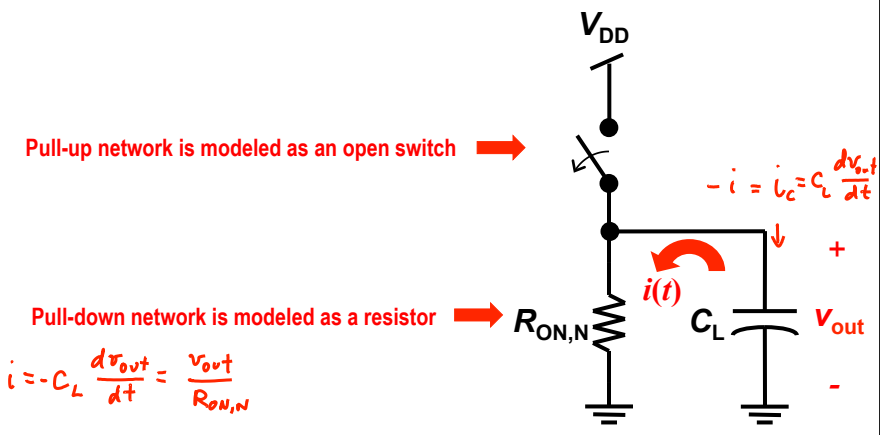
RC Circuit Model for High-Low Transition

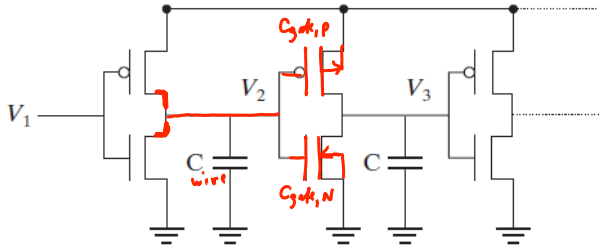
Initially $V_{out} = V_{DD}$; then NMOSFET(s) connect(s) V_{out} to GND:



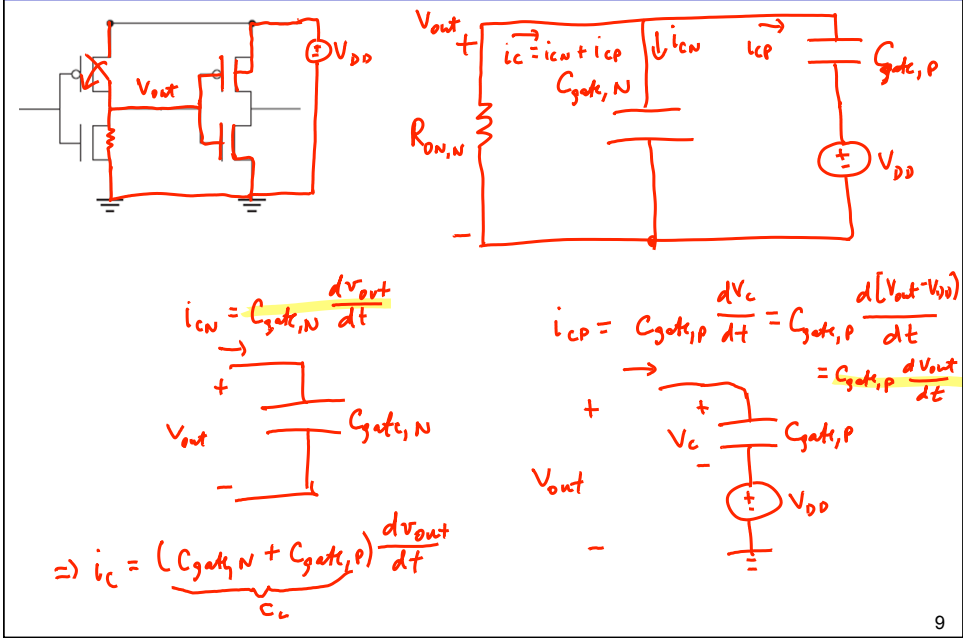
Output Load Capacitance of a Logic Gate

- **The output load capacitance of a logic gate comprises several components:**
  - **pn-junction capacitance**
    for both NMOS and PMOS transistors
  - **capacitance of connecting wires**
  - **input capacitances of the "fan-out" gates**

★ $C_{gate,N}$, $C_{gate,P}$



Derivation of RC Model



Derivation of $V_{out}(t)$ for High-Low Transition

Approach #1: By separation of variables $\quad v_{out} = -RC \frac{dv_{out}}{dt}$

$$dt = -RC \left(\frac{1}{v_{out}}\right) dv_{out}$$

$$\int dt = -RC \int \frac{1}{v_{out}} dv_{out}$$

$$t + C_1 = -RC \ln v_{out} \quad \Rightarrow -\frac{t}{RC} + \frac{C_1}{RC} = \ln v_{out}$$

C_1: constant

$$\Rightarrow v_{out} = \exp\left(-\frac{t}{RC} + \frac{C_1}{RC}\right) = e^{-t/RC} e^{C_1/RC} = C e^{-t/RC}$$

Initial Condition: At $t = 0$, $v_{out} = V_{DD} = C$

$$\boxed{v_{out}(t) = V_{DD} e^{-t/RC}}$$

Derivation of $V_{out}(t)$ for High-Low Transition

Approach #2: With eigenfunctions

$v_{out} = -RC\frac{dv_{out}}{dt}$

$v_{out} = -RC\,f(v_{out})$

$-\frac{1}{RC}v_{out} = f(v_{out})$ → v_{out} is an eigenfunction of $f(\cdot)$

Only an exponential function has a derivative proportionate to itself

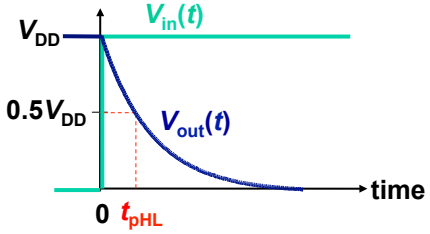
→ $v_{out} = K e^{t/\tau}$ (K: scalar factor) where τ is a constant "time constant"

Plug into Diff. Eqn.: $K e^{t/\tau} = -RC\frac{d}{dt}(Ke^{t/\tau}) = -RC\left(\frac{K}{\tau}\right)e^{t/\tau}$

$\Rightarrow -\frac{RC}{\tau} = 1 \Rightarrow \tau = -RC$ $\quad v_{out} = Ke^{-t/RC} = V_{DD}e^{-t/RC}$ (K: initial condition)

Derivation of Formula for t_{pHL}

$$v_{out}(t) = V_{DD}e^{-t/R_{ON,N}C_L}$$



At $t = t_{pHL}$:

$v_{out} = \frac{V_{DD}}{2} = V_{DD}e^{-t_{pHL}/RC}$

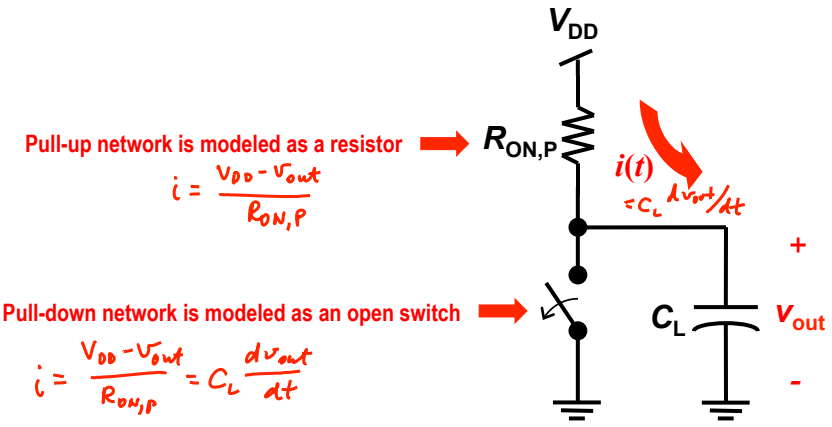
$\frac{1}{2} = e^{-t_{pHL}/RC} \Rightarrow 2 = e^{t_{pHL}/RC}$

$\ln(2) = t_{pHL}/RC$

$\Rightarrow t_{pHL} = RC\ln(2) = 0.69RC$

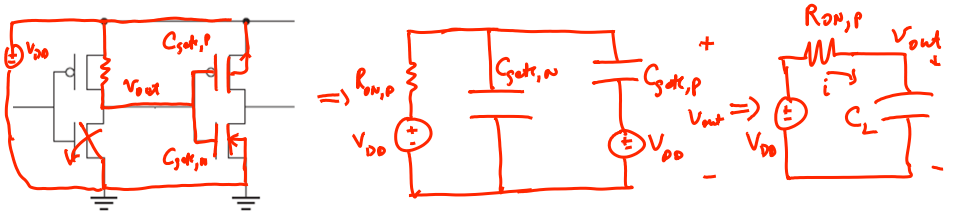
RC Circuit Model for Low-High Transition

Initially $V_{out} = 0$; then PMOSFET(s) connect(s) V_{out} to V_{DD}:

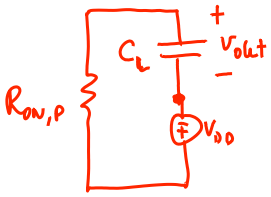


$$V_{DD} - v_{out} = R_{ON,P} C_L \, dv_{out}/dt$$

Derivation of RC Model



Redraw:



Define $v'_{out} = v_{out} - V_{DD}$

+

v'_{out}

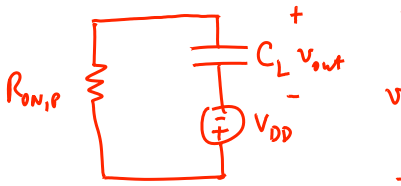
-

Solution to Diff Eqn is the same as before since $\frac{dv'_{out}}{dt} = \frac{d(v_{out} - V_{DD})}{dt} = \frac{dv_{out}}{dt}$

Derivation of $V_{out}(t)$ for Low-High Transition

Initially, $v_{out} = 0$ and

$v_{out}' = 0 - V_{DD} = -V_{DD}$



$v_{out}' = v_{out} - V_{DD}$

$$v_{out}' = v_{out}'(t=0)\, e^{-t/R_{ON,P}C_L}$$

$$v_{out} - V_{DD} = -V_{DD} e^{-t/R_{ON,P}C_L}$$

$$v_{out} = V_{DD}\left[1 - e^{-t/R_{ON,P}C_L}\right]$$

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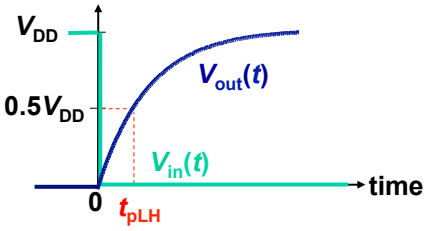
Derivation of Formula for t_{pLH}

$$v_{out}(t) = V_{DD}\left(1 - e^{-t/R_{ON,P}C_L}\right)$$



At $t = t_{pLH}$:

$$v_{out} = \frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-t_{pLH}/RC}\right)$$

$$e^{-t_{pLH}/RC} = \frac{1}{2} \Rightarrow e^{t_{pLH}/RC} = 2$$

$$t_{pLH}/RC = \ln(2)$$

$$t_{pLH} = \ln(2)RC = 0.69RC$$

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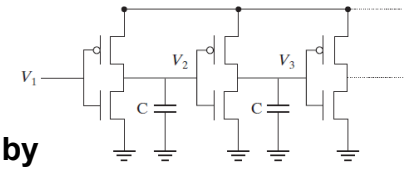
Minimizing Propagation Delay



A fast CMOS logic circuit is built by

1. **Keeping the output capacitance C_L small**
   - → Minimize the area of drain pn junctions.
   - → Lay out devices to minimize interconnect capacitance.
   - → Avoid large fan-out.
2. **Decreasing the equivalent resistance of the transistors**
   - → Decrease gate length L_G
   - → Increase transistor width W
     - … but this increases pn junction area and hence C_L
3. **Increasing V_{DD}**
   - → trade-off with power consumption…

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Classroom Analogy