EE247
Lecture 14

- Administrative issues:
  - Midterm date changed to Thurs. Oct. 21
  - Final exam moved to Wednesday, December 15, 12:30-3:30pm
  - Both date changes due to conflict with EE142
  - No homework next week

EE247
Lecture 14

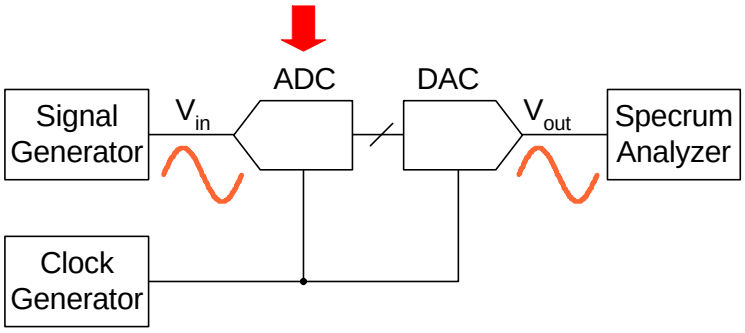
- Data Converters
  - Practical aspects of converter testing
    - Signal source
    - Clock generator
    - Evaluation board considerations
  - D/A converter design

Converter Testing
Practical Aspects

Just Got Silicon Back...

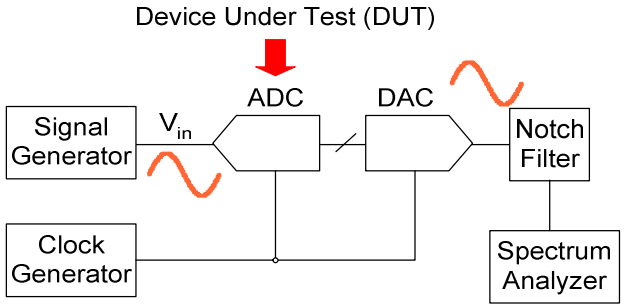
- Now what ?
- Practical aspects of converter testing
- Equipment requirements
- Pitfalls

Direct ADC-DAC Test



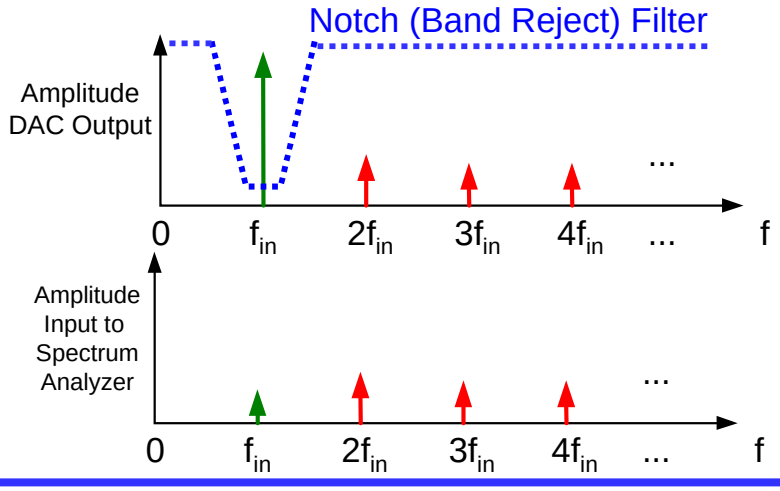
- Need a very good DAC
- Actually a good way to "get started"...

Direct ADC-DAC Test

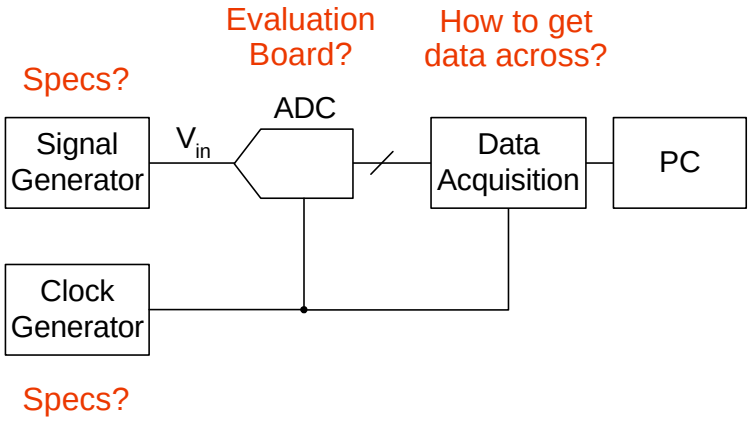


- Beware of spectrum analyzer nonlinearities
- For high performance converter linearity test, may need to notch out the signal to measure the ADC linearity via spectrum analyzer
- Need to build or purchase notch filter/s

Filtering



ADC Test Setup



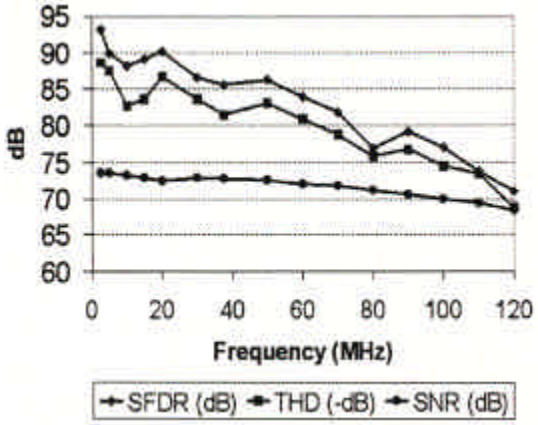
Example: High Performance ADC

Resolution	14 bits
Conversion Rate	75 MSPS
Input Range	2 V_{pp} differential
SNR @ Nyquist	73 dB
SFDR @ Nyquist	88 dB
DNL	0.6 LSB
INL	2.0 LSB

[W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits,* Dec. 2001]

- Testing a high performance converter may be just as challenging as designing it!
- Key to success is to be aware of test setup and equipment limitations

Example: ADC Linearity Test



Ref: W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits,* Dec. 2001

Signal Source

- Need: SFDR>95dB @ $f_{in}=f_s/2=37.5$MHz & SFDR>70dB to about 120MHz
- Let's see, how about the "value priced" signal generator available in most labs...

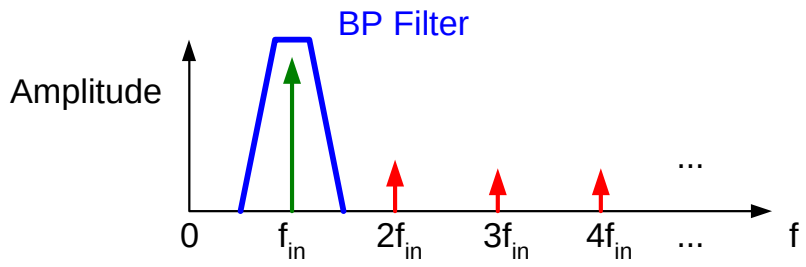
- f=0...15MHz
- Harmonic distortion (f>1MHz): -35dBc
  → Does not cover the required frequency range & poor linearity

A Better Signal Source

- OK, now we've spent about $40k, this should work now... (?)

- f=100kHz...3GHz
- Harmonic distortion (f>1MHz): -30dBc !
- No way to produce the sine wave we need without a filter!

Filtering Out Harmonics



- Given HD=-30dBc, we need a stopband rejection > 65dB to get SFDR>95dB

Available Filters

Elliptical Function Bandpass Filters 1kHz to 20MHz

www.tte.com, or
www.allenavionics.com

Stopband to Passband Bandwidth Ratios

Series Number	BWR	*Stopband Attenuation
Q34	4.0:1	-40dBc
Q40	4.0:1	-40dBc
Q36	10.0:1	-60dBc
Q54	2.5:1	-40dBc
Q70	3.5:1	-60dBc
Q56	3.5:1	-60dBc

- Want to test at many frequencies → Need to have at least one filter per test frequency!

Tunable Filter

www.klmicrowave.com

K&L Model	Frequency Range (MHz)	Passband Insertion Loss	Length Inch/mm	Width Inch/mm	Height Inch/mm
5BT-30/76-5-N/N	30-76	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-63/125-5-N/N	63-125	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-125/250-5-N/N	125-250	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-250/500-5-N/N	250-500	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-375/750-5-N/N	375-750	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-500/1000-5-N/N	500-1000	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-750/1500-5-N/N	750-1500	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-1000/2000-5-N/N	1000-2000	1.0 dB Max	7.38/187	2.88/73	2.75/50
5BT-1200/2600-5-N/N	1200-2600	1.0 dB Max	7.38/187	2.88/73	2.75/50

Filter Distortion

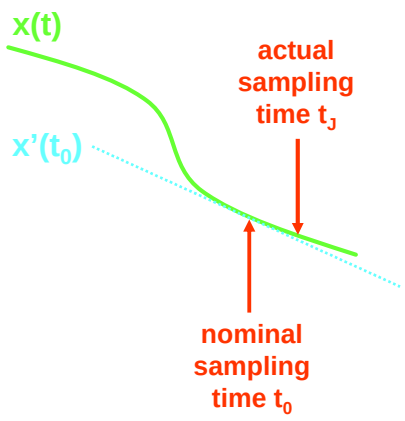
- Beware: The filters themselves also introduce distortion
- Distortion is usually not specified, need to call manufacturer
- Often guaranteed: HD<-85dBc,
- Don't trust your filters blindly...

Clock Generator

- Let us check if for the clock a "value-priced" signal generator will suffice...
- No! The clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)
- Variability in T causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"
- How much Jitter can we tolerate?

Clock Jitter

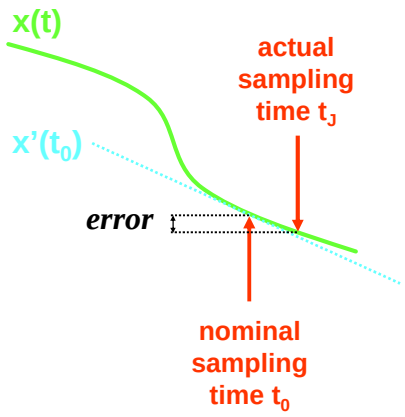
- Sampling jitter adds an error voltage proportional to the product of (t_J-t_0) and the derivative of the input signal at the sampling instant
- Jitter doesn't matter when sampling dc signals ($x'(t_0)=0$)



Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$



Jitter Example

Sinusoidal input

$Amplitude: \quad A$
$Frequency: \quad f_x$
$Jitter: \quad dt$

$$x(t) = A\sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x A\cos(2\pi f_x t)$$

$$|x'(t)|_{max} \le 2\pi f_x A$$

$$|e(t)| \le |x'(t)|dt$$

$$|e(t)| \le |2\pi f_x A|dt$$

Worst case

$$A = A_{FS}/2 \qquad f_x = f_s/2$$

$$e(t) \le \pi f_s A_{FS}/2\, dt$$

$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$

$$dt << \frac{1}{2^B \pi f_s}$$

# of Bits	f_s	dt <<
16	10 MHz	0.5 ps
12	100 MHz	0.8 ps
8	1000 MHz	1.2 ps

Law of Jitter

- The worst case looks pretty stringent …
  what about the "average"?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal

  $x(t) = A\sin(2\pi f_x t)$,

  then
  - $x'(t) = 2\pi f_x A\cos(2\pi f_x t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance $E\{(t_J - t_0)^2\} = \tau^2$

Law of Jitter

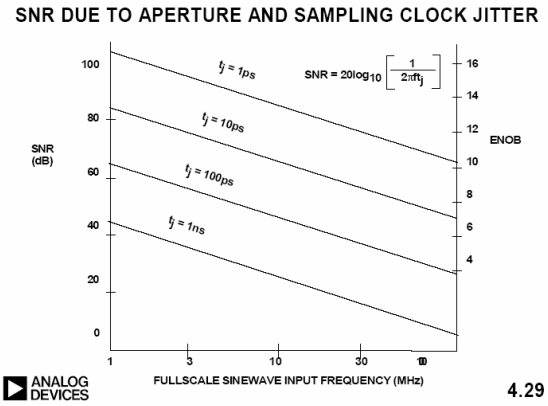
- If $x'(t)$ and the jitter are independent
  - $E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\}\, E\{(t_J - t_0)^2\}$
- Hence, the jitter error power is

  $E\{e^2\} = 2p^2 f_x^2 A^2 t^2$ (compare to the worst case $4\pi^2 f_x^2 A^2 t^2$)
- If the jitter is uncorrelated from sample to sample, this "jitter noise" is white

Law of Jitter

$$DR_{\text{jitter}} = \frac{A^2/2}{2p^2 f_x^2 A^2 t^2} = \frac{1}{2p^2 f_x^2 t^2} = -20\log_{10}(2pf_x t)$$

ADC under test:
SNR=73dB
f_{in}=37.5MHz
$\Rightarrow \tau$<<1ps rms !



More on Jitter

- Once we have a good enough generator, other circuit and test setup related issues may determine jitter, but...
- Usually, clock jitter in the single-digit pico-second range can be prevented by appropriate design techniques
  - Separate supplies
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input frequency
  - RMS noise proportional to input amplitude

  →In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...

Evaluation Board

- Planning begins with converter pin-out
  - Example of poor pin-out→ clock pin right next to a digital output...
- Not "Black Magic", but weeks of design time and learning
- Key aspects
  - Supply/ground routing, bypass capacitors
  - Coupling between signals
- Good idea to look at ADC vendor datasheets for example layouts/schematics/application notes

Vendor Eval Board Layout

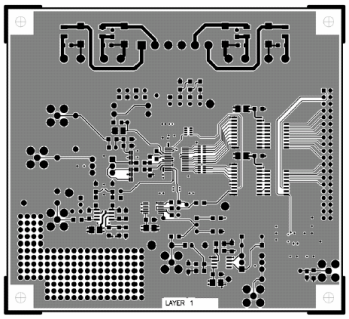


Figure 21. TSSOP Evaluation Board Layout, Primary Side

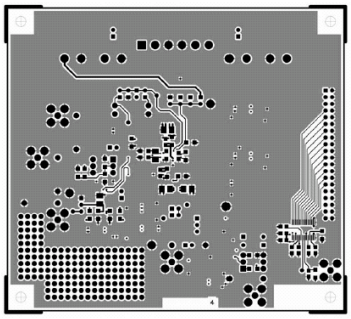


Figure 22. TSSOP Evaluation Board Layout, Secondary Side

[Analog Devices AD9235 Data Sheet]

Issues

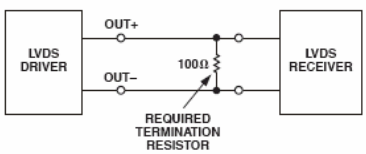
- A converter does not just have one "input"
  - Clock
  - Power Supply, Ground
  - Reference Voltage
- For good practices on how to avoid issues see e.g.:
  - Analog Devices Application Note 345**:** "Grounding for Low-and-High-Frequency Circuits"
  - Maxim Application Note 729**:** "Dynamic Testing of High-Speed ADCs, Part 2"

How to Get the Bits Off Chip?

- "Full swing" CMOS signaling works well for f_{CLK}<100MHz
- But we want to build faster ADCs...
- Alternative to CMOS: LVDS – Low Voltage Differential Signaling
- LVDS vs. CMOS:
  - Higher speed, more power efficient at high speed
  - Two pins/bit!

LVDS Outputs

Figure 1. LVDS Output Levels



Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

LVDS Outputs

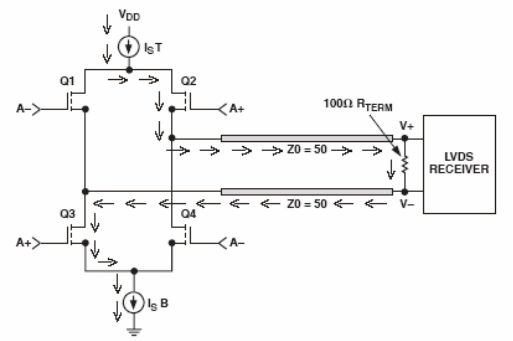
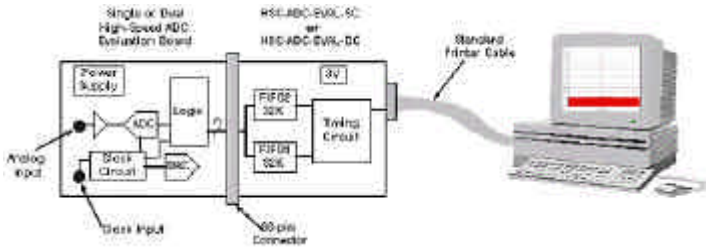


Figure 4. LVDS Output Current

Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

Data Acquisition

- Several options:
  - Logic analyzer with PC interface
  - FIFO board, interface to PC DAQ card
  - Vendor kit, simple interface to printer port:

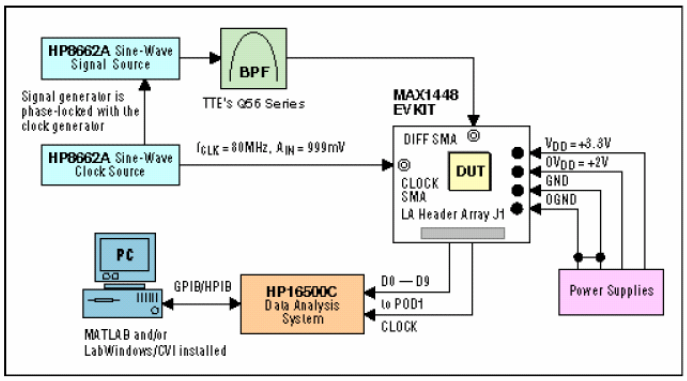


[Analog Devices, High-Speed ADC FIFO Evaluation Kit]

Post-Processing

- LabView (DAQ Software Toolbox)
- Matlab
- Some vendors provide example source code
- E.g. Maxim Application Note 1819**:** "Selecting the Optimum Test Tones and Test Equipment for Successful High-Speed ADC Sine Wave Testing"
- EE247 Matlab Examples, e.g. Sine Code Density Test

Complete Setup



[Maxim Application Note 729**:** "Dynamic Testing of High-Speed ADCs, Part 2]

Debugging

- State-of-the-art converters almost always yield surprises in silicon
  - If models anticipate everything, the application probably isn't state-of-the-art
- Analog designers and mixed-signal architects often invent new circuits while measuring in the lab
- How do we debug converters?
  - Start with a simple time domain test. Does the captured digital waveform look like a sine wave?
  - Begin your DFT/INL signature analysis by scaling down sampling frequencies and signal input frequencies together
  - If you can't explain performance with essentially infinite settling times, don't add dynamic errors to the mix

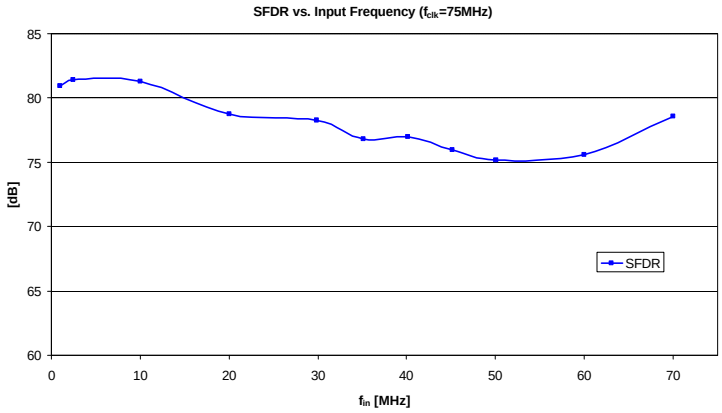
Debugging

- Typical problems come from non-idealities never built into your "model"
  - E.g. half-circuit models for fully-differential circuits inherently can't explain some types of differential-symmetry errors
- You can't afford to rediscover old non-idealities in new silicon
  - Talking to veterans early in the modeling phase can be important

Debugging

- Design teams usually track down and fix single-cause problems quickly
- Interactions are much trickier
- Interaction examples:
  - Digital activity-dependent clock jitter
    - S/(N+D) degradation only happens when large amplitude, high frequency analog inputs coincide with the offending digital activity
  - Distortion cancellation
    - Nonlinear phenomena don't obey superposition

Debugging



- Cancellation of Nonlinearities?

Debugging

- Never assume all of your data is good
  - One bad data set can “rule out” the correct explanation, leading you astray forever
- "Compare measurements to themselves“
- But, noise is a random variable, and the noise power in 1000 time samples will vary from DFT to DFT
- How big an effect is this?

Debugging

- Can show that:
  - Variation of noise in 1000 samples yields a standard deviation in SNR of 0.2dB
  - This means that 68.3% of all DFTs will produce SNRs within 0.2dB of the average
  - 99.7% of 1000 point DFTs yield SNRs within ±0.6dB of the average
- If you're seeing ADC noise variation of greater than ±0.6dB in the lab, some sort of interference is usually the culprit

Debugging

- Always try to use two independent measurement methods to verify important results
  - Correlate INL & SFDR, DNL & SNR
- Comparing time domain and frequency domain views of the same measurement is good practice
  - DC histogram test & thermal noise - DNL & SNR

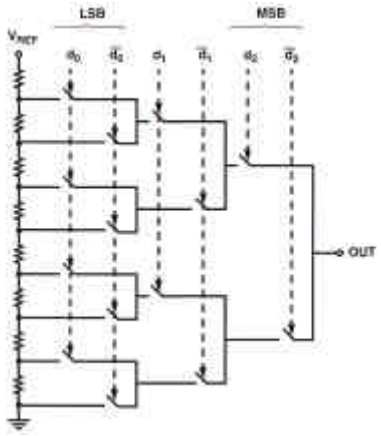
D/A Converters

- D/A architecture examples
  - Unit element
  - Binary weighted
- Static performance
  - Component matching
  - Architectures
    - Unit element
    - Binary weighted
    - Segmented
  - Dynamic element matching
- Dynamic performance
  - Glitches
- DAC Examples

D/A Examples

- Voltage, Charge, or Current Based
- E.g.
  - Resistor string
  - Charge redistribution
  - Current source type

R-String DAC



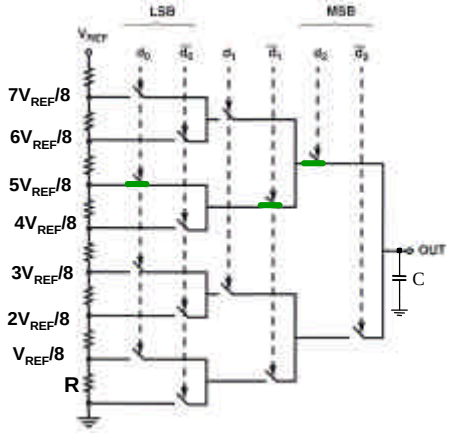
R-String DAC Example

Example:
Input code 101

→ $V_{out} = 5V_{REF}/8$

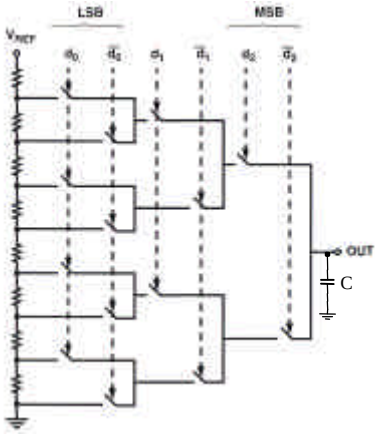
$\tau_{settling}$ =

=(3R||5R) x C
=0.23 x 8RC



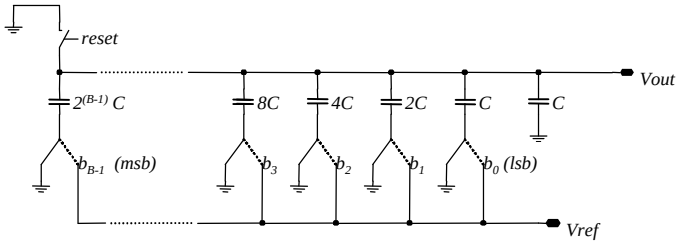
R-String DAC

- Advantages:
  - Simple, fast for <8-10bits
  - Inherently monotonic
  - Compatible with purely digital technologies
- Disadvantages:
  - 2^B resistors & 2^B switches for B bits → High element count & larger area for B>10bits
  - High settling time for B > 10: $\tau_{max} = 0.25 \times 2^B RC$



*Ref: M. Pelgrom, "A 10-b 50-MHz CMOS D/A Converter with 75-W Buffer," JSSC, Dec. 1990, pp. 1347.

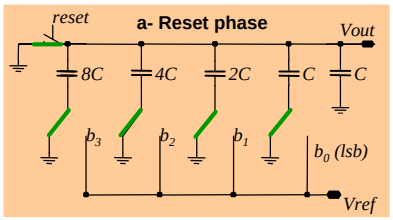
Charge Redistribution DAC

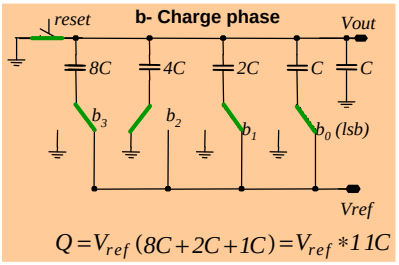


$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C} V_{ref}$$

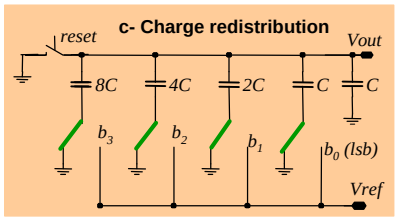
- E.g. "Binary weighted"
- B+1 capacitors & switches (if unit elements used 2^B caps)

Charge Redistribution DAC
Example: 4Bit DAC- Input Code 1011





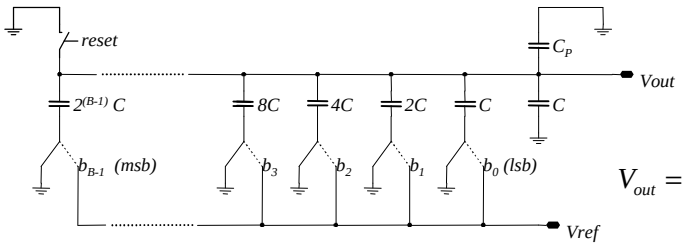
$$Q = V_{ref}(8C + 2C + 1C) = V_{ref} * 11C$$



$$V_{ref} * 11C = V_{out} * 16C$$

$$\rightarrow V_{out} = \frac{11}{16} V_{ref}$$

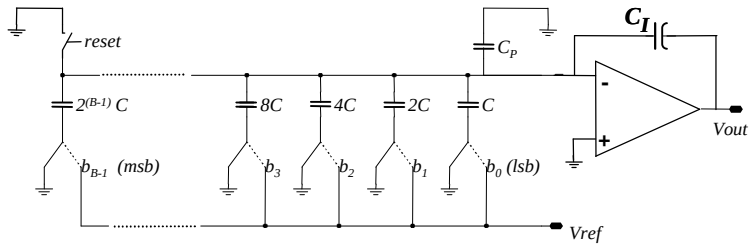
Charge Redistribution DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C + C_P} V_{ref}$$

- Monotonicity depends on element matching
- Large area of caps for high DAC resolution (10bit DAC ratio 1:512)
- Sensitive to parasitic capacitor @ output

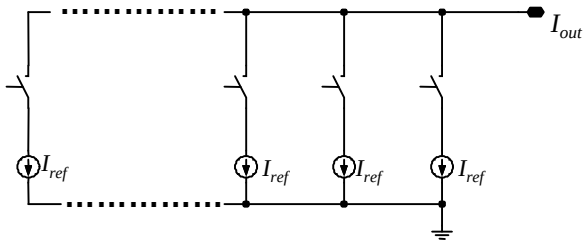
Charge Redistribution DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{C_I} V_{ref}$$

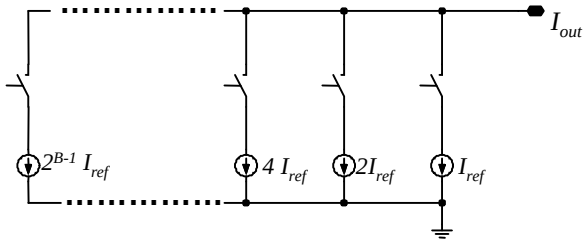
- Opamp helps eliminate the parasitic capacitor effect
  - Issue: opamp offset & speed

Current Source DAC Unit Element



- "Unit elements "
- Monotonicity does not depend on element matching
- 2^B-1 current sources & switches

Current Source DAC Binary Weighted



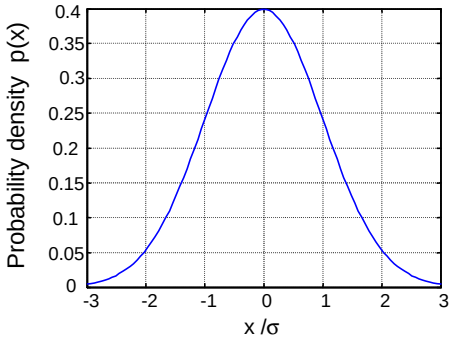
- "Binary weighted"
- Monotonicity depends on element matching
- B current sources & switches (2^B-1 unit elements)

Static DAC INL / DNL Errors

- Component matching
- Systematic errors
  - Contact resistance
  - Edge effects in capacitor arrays
  - Process gradient
  - Finite current source output resistance
- Random errors
  - Lithography
  - Often Gaussian distribution (central limit theorem)

*Ref: C. Conroy et al, "Statistical Design Techniques for D/A Converters," JSSC Aug. 1989, pp. 1118-28.

Gaussian Distribution



$$p(x)=\frac{1}{\sqrt{2p}\,s}e^{-\frac{(x-m)^2}{2s^2}}$$

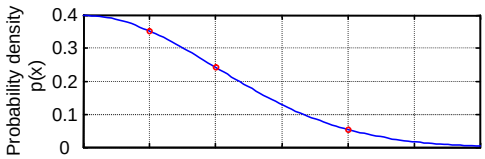
$$where\ standard\ \ deviation: s=\sqrt{E(X^2)-m^2}$$

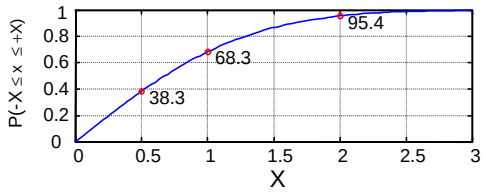
Yield

$$P(-X\le x\le +X)=$$

$$=\frac{1}{\sqrt{2p}}\int_{-X}^{+X}e^{-\frac{x^2}{2}}dx$$

$$=erf\left(\frac{X}{\sqrt{2}}\right)$$





Yield

X/s	P(-X £ x £ X) [%]	X/s	P(-X £ x £ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937