EE247
Lecture 18

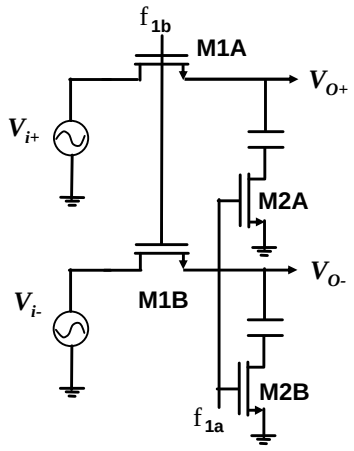
ADC Converters

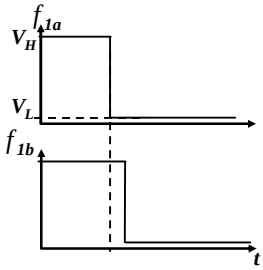
- Sampling switch charge injection
  - Bottom plate sampling
  - Flip around track & hold
  - Sample and hold including gain
  - Sample and hold including offset cancellation
- Impact of ESD protection on converters
- ADC architectures

Sampling Switch Charge Injection Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Charge sharing with C_{ov}
  - Channel charge transfer
- Issues:
  - DC offset
  - Input dependant error voltage → distortion
- Solutions:
  - Complementary switch→ only cancels offset, does not address input signal dependant error
  - Addition of dummy switches→ cancels charge injection to 1st order but not fully
  - Bottom-plate sampling?

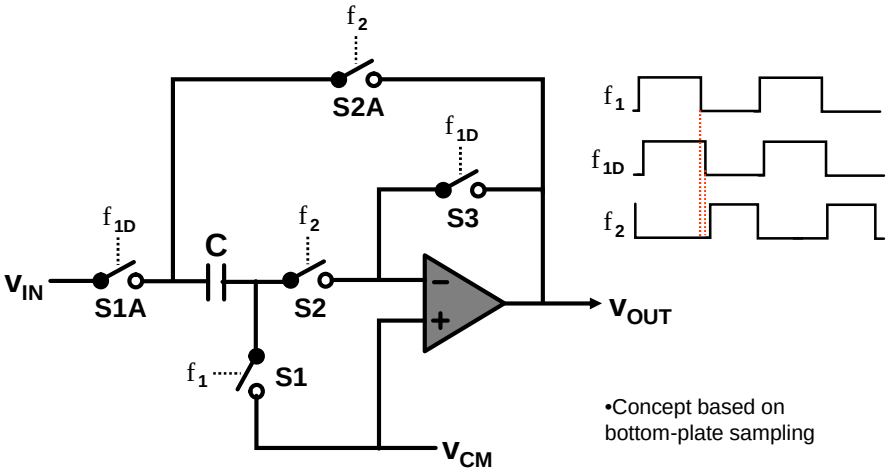
Switch Charge Injection Bottom Plate Sampling





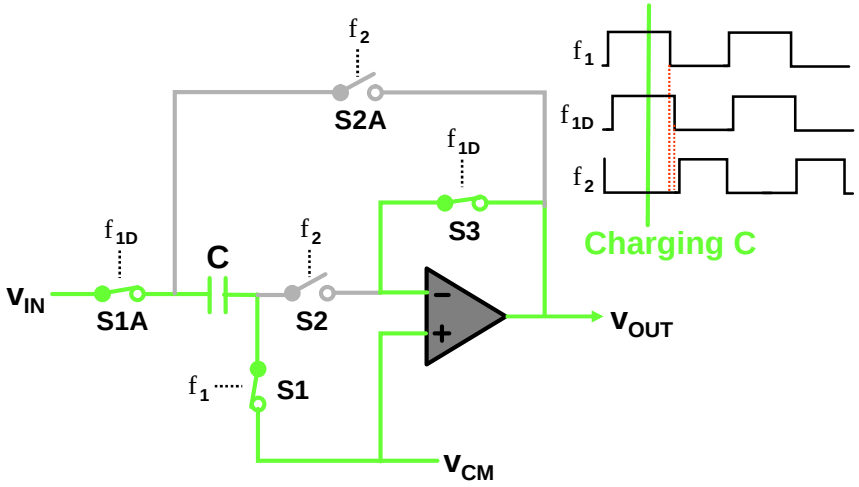
- Switches M2A@ B are opened slightly earlier compared to M1A&B
  - → Injected charge by the opening or M2AB is constant & eliminated when used differentially
- Since bottom plate of C_s is open when M1A&B are opened→ no charge injected on C_s

Flip-Around T/H

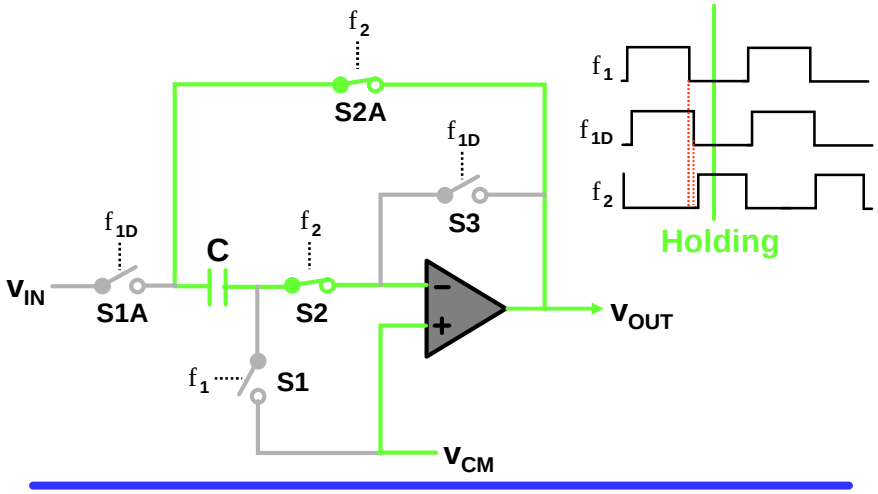


- Concept based on bottom-plate sampling

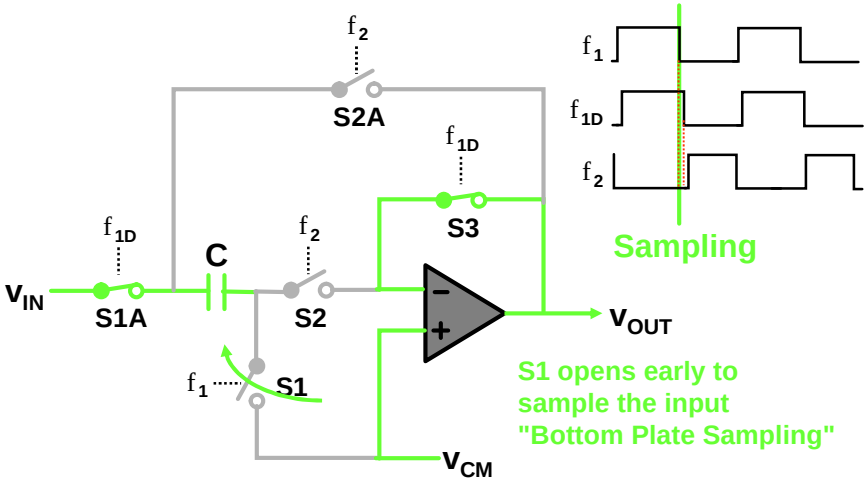
Flip-Around T/H



Flip-Around T/H



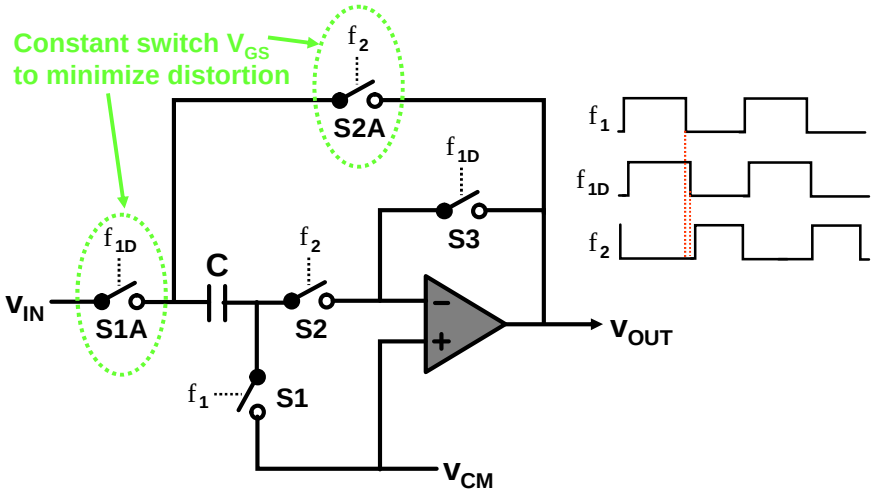
Flip-Around T/H - Timing



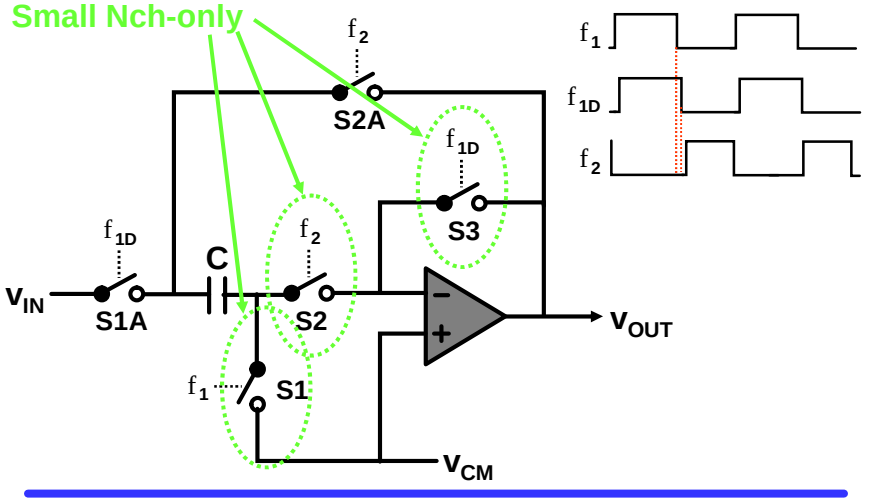
Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C
- With "Bottom Plate Sampling", charge injection comes only from S1 and is to first-order independent of v_{IN}
  - Only a dc offset is added to the input signal
  - This dc offset can be removed with a differential architecture

Flip-Around T/H



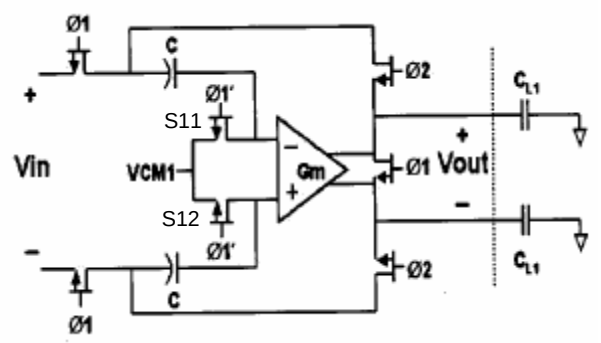
Flip-Around T/H



Flip-Around T/H

- S1 is an n-channel MOSFET
- Since it always switches the same voltage, it's on-resistance, R_{S1}, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - S1A is a wide (much lower resistance than S1) constant V_{GS} switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A's resistance is negligible → delay depends only on S1 resistance
  - S1 resistance is independent of v_{IN} → delay is independent of v_{IN}

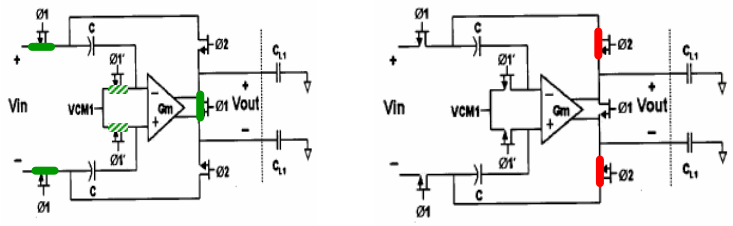
Differential Flip-Around T/H

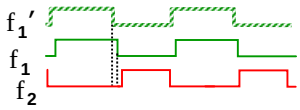


Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit

Ref: W. Yang, *et al.* "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001 1931

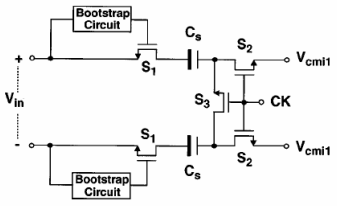
Differential Flip-Around T/H

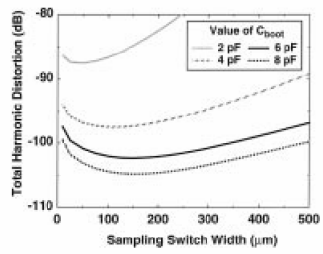




- Gain=1
- Feedback factor=1
- $\Delta V_{in\text{-}cm}=V_{out\_com}-V_{sig\_com}$
  - → Amplifier needs to have large input common-mode compliance

Differential Flip-Around T/H
Choice of Sampling Switch Size

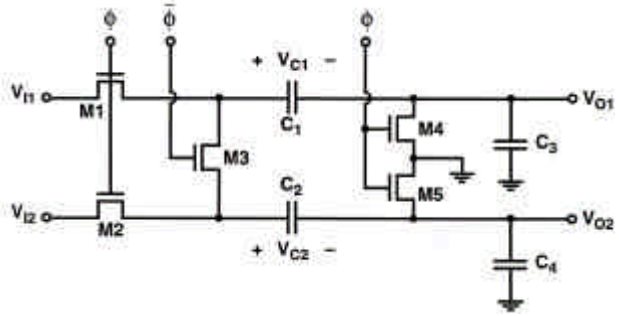




- THD simulated w/o sampling switch boosted clock → -45dB
- THD simulated with sampling switch boosted clock (see figure)

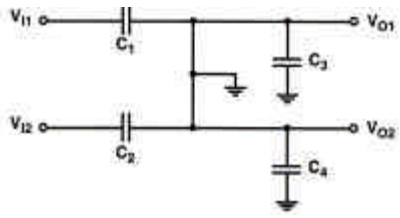
Ref: K. Vleugels et al, "A 2.5-V Sigma–Delta Modulator for Broadband Communications Applications "
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887

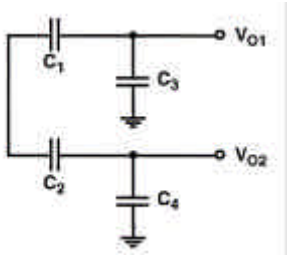
Input Common-Mode Cancellation



Ref: R. Yen, *et al.* "A MOS Switched-Capacitor Instrumentation Amplifier,"
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6,, DECEMBER 1982 1008

Input Common-Mode Cancellation



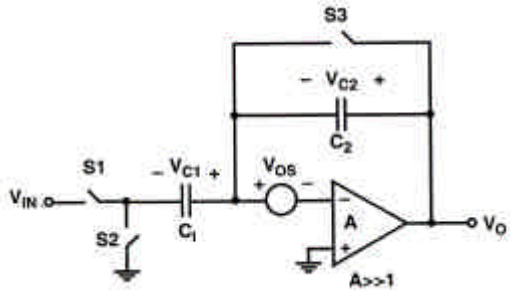


Track mode (ϕ high)
$V_{C1}=V_{I1}$, $V_{C2}=V_{I2}$
$V_{o1}=V_{o2}=0$

Hold mode (ϕ low)
$V_{o1}+V_{o2}=0$
$V_{o1}-V_{o2}= -(V_{I1}-V_{I2})(C_1/(C_1+C_3))$

→ Input common-mode level removed

S/H + Charge Redistribution Amplifier



Track mode (S1, S3 →on S2→ off)
$V_{C1}=V_{os}-V_{IN}$, $V_{C2}=0$
$V_o=V_{os}$

S/H + Charge Redistribution Amplifier Cont'd

$$V_{C1} \longrightarrow V_{os}$$

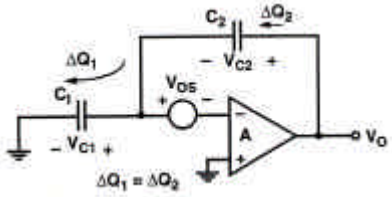
$$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$$

$$\Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN}$$

$$\Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1$$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right) V_{C1} = V_{C2}$$

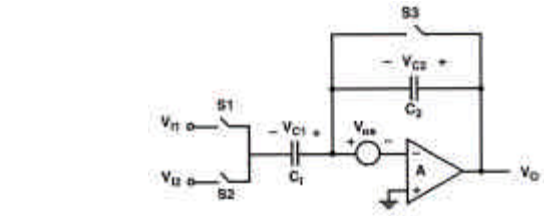
$$V_O = V_{C2} + V_{os} = \left(\frac{C_1}{C_2}\right) V_{IN} + V_{os}$$

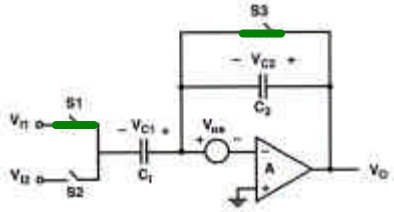


Hold/amplify mode (S1, S3 →off S2→ on)

→Offset NOT cancelled, but not amplified
→Input-referred offset =(C_2/C_1)xV_{OS}, & C_2<C_1

S/H & Input Difference Amplifier

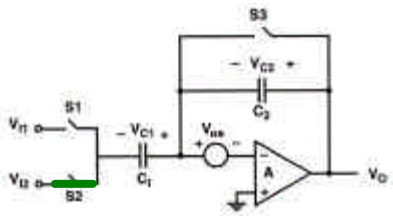




Sample mode (S1, S3 →on S2→ off)
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$

Input Difference Amplifier Cont'd

Subtract/Amplify mode (S1, S3 →off S2→ on)
During previouse phase:
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$



$$V_{C1} = V_{os} - V_{I2}$$

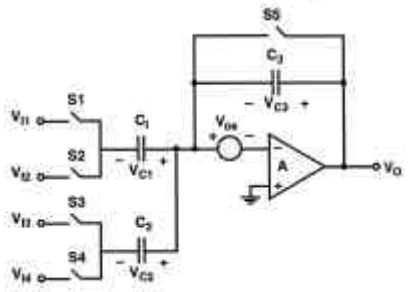
$$\Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C1} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$$

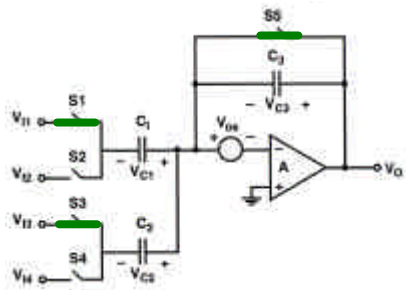
$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$

→Offset NOT cancelled, but not amplified
→Input-referred offset =$(C_2/C_1)xV_{OS}$, & $C_2<C_1$

S/H & Summing Amplifier



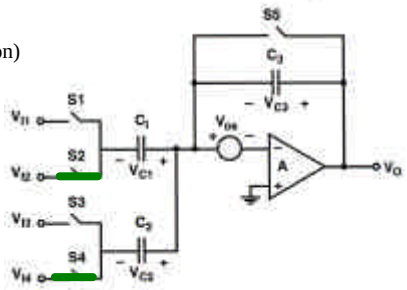
S/H & Summing Amplifier Cont'd



Sample mode (S1, S3, S5→on S2, S4→ off)
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=V_{os}-V_{I3}$, $V_{C3}=0$
$V_o=V_{os}$

S/H & Summing Amplifier Cont'd

Amplify mode (S1, S3, S5→off, S2, S4→ on)



$$V_{C1} = V_{os} - V_{I2} \Rightarrow \Delta V_{C1} = V_{I1} - V_{I2}$$

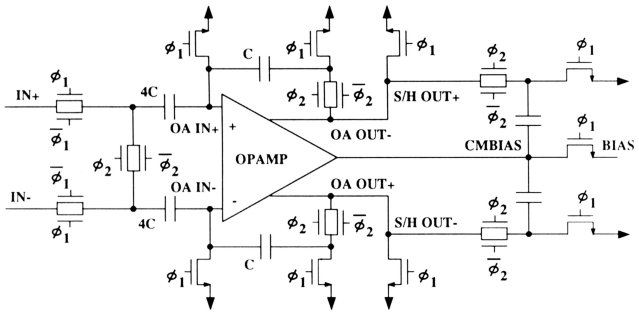
$$V_{C2} = V_{os} - V_{I4} \Rightarrow \Delta V_{C2} = V_{I3} - V_{I4}$$

$$\Delta Q_3 = \Delta Q_1 + \Delta Q_2 = C_1 \Delta V_{C1} + C_2 \Delta V_{C2}$$

$$\Delta V_{C3} = \frac{\Delta Q_3}{C_3} = \left(\frac{C_1}{C_3}\right)(V_{I1} - V_{I2}) + \left(\frac{C_2}{C_3}\right)(V_{I3} - V_{I4})$$

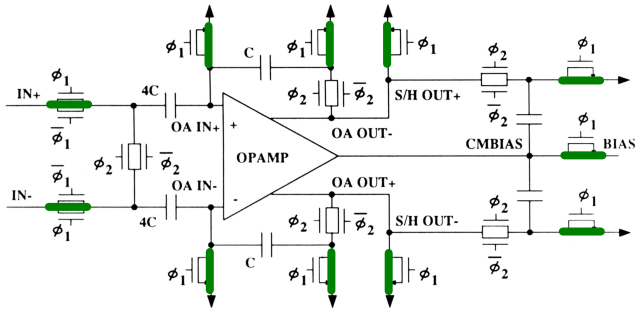
$$V_O = \left(\frac{C_1}{C_3}\right)(V_{I1} - V_{I2}) + \left(\frac{C_2}{C_3}\right)(V_{I3} - V_{I4}) + V_{os}$$

Differential S/H Combined with Gain Stage



Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential S/H Combined with Gain Stage



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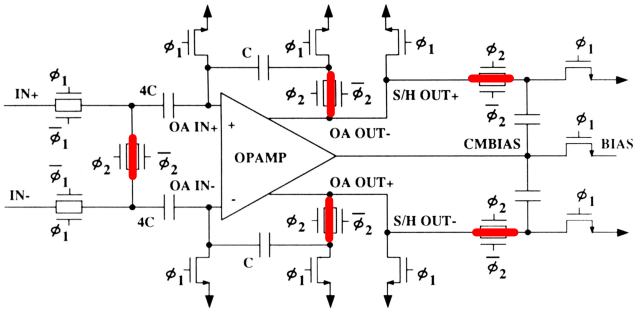
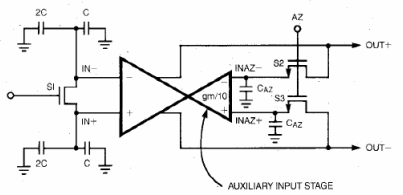
Differential S/H Combined with Gain Stage



- *Gain=4C/C=4*
- *Feedback factor =1/(1+G)=0.2*
- *Input common-mode level removed*
- *Amplifier offset not removed*

Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential S/H Including Offset Cancellation

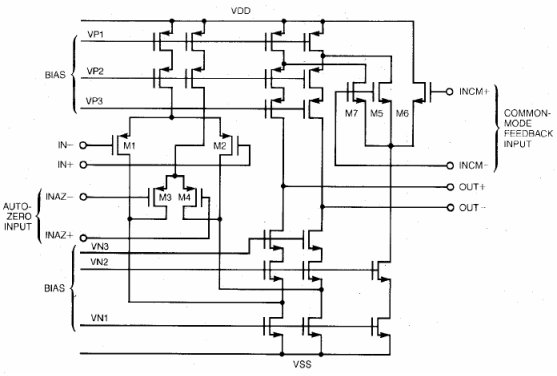


- Operation during offset cancellation shown
- Auxilary inputs added with A_{main}/A_{aux}.=10
- During offset cancellation phase AZ and S1 closed → main amplifier offset stored on C_{AZ}
- Auxiliary amp chosen to have lower gain so that aux. amp offset & charge injection associated with opening of switch AZ → reduced by A_{aux}/A_{main}=1/10
- Requires an extra auto-zero clock phase

Ref: H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

Differential S/H Including Offset Cancellation Operational Amplifier

- Operational amplifer → dual input folded-cascode opamp
- M3,4 auxilary input, M1,2 main input
- To achieve 1/10 gain ratio $W_{M3,4}$ =1/10x $W_{M1,2}$ & current sources are scaled by 1/10
- M5,6,7 → common-mode control
- Output stage → dual cascode → high DC gain

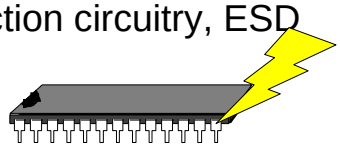


Ref: H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

ESD Protection
ADC Architectures

What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events are destructive



Model and Protection Circuit

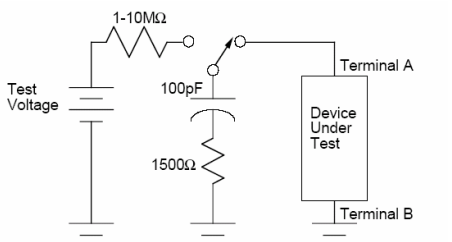
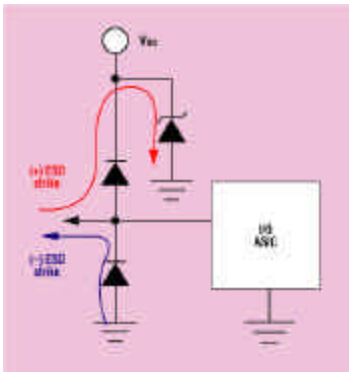


Figure 1. Human Body Model for ESD testing.



[http://www.ce-mag.com/archive/03/ARG/dunnihoo.html]

Equivalent Circuit

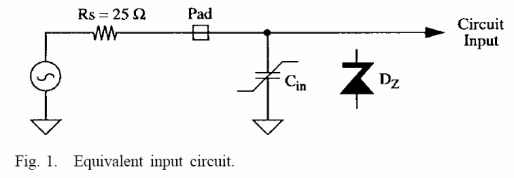
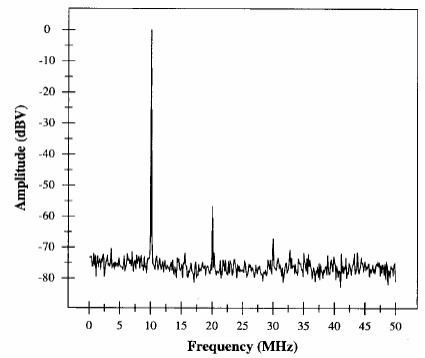


Fig. 1. Equivalent input circuit.

[I. E. Opris, "Bootstrapped pad protection structure," IEEE J.Solid-State Circuits, pp. 300, Feb. 1998.]

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!

ESD Circuit Distortion

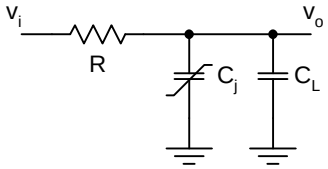


[I. E. Opris, "Bootstrapped pad protection structure," IEEE J.Solid-State Circuits, pp. 300, Feb. 1998.]

$C(V_{in})$= 2..4pF for V_{in}=2..0V

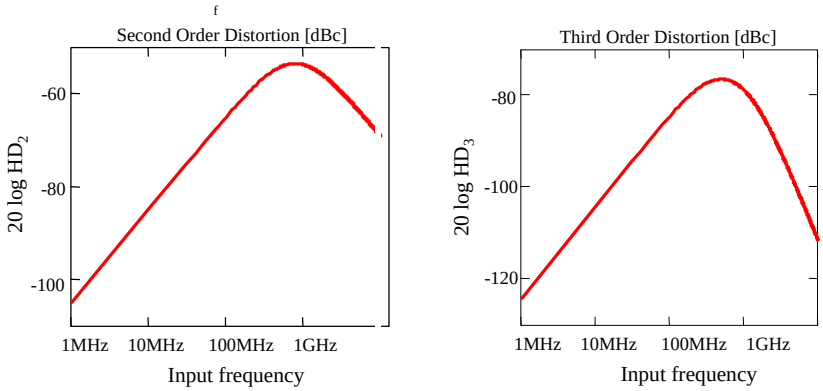
ESD Circuit Distortion

- Analysis:
  - Model nonlinear cap & run SPICE
  - Hand calculations using Volterra Series
- Example:



R=25Ω
C_{jo}=1pF
C_L=5pF
V_{ipeak}=0.5V

ESD Circuit Distortion



HD3(37.5MHz) = -92dB

HD3(100MHz) = -84dB

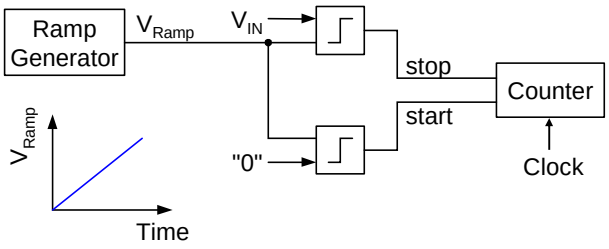
ESD Circuit Distortion

- Distortion from ESD circuits approaches state of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Ref.: A. Wang, "Recent developments in ESD protection for RF IC," *Proc. DAC Conference*, Jan. 2003
- Solutions still pre-mature
- Lots of company IP

ADC Architectures

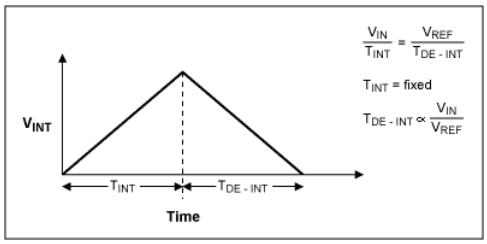
- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - …
- Oversampled ADCs

Single Slope ADC



- Low complexity
- Hard to generate precise ramp
- Better: Dual Slope, Multi-Slope

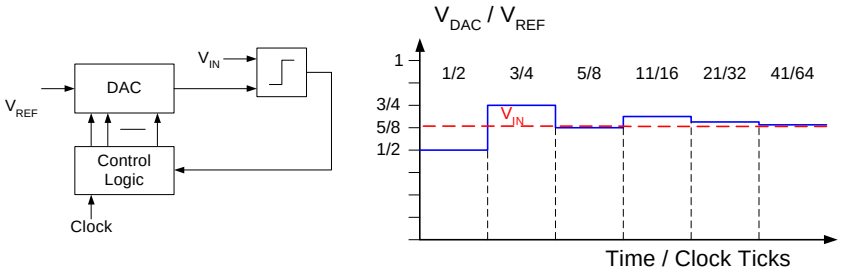
Dual Slope ADC



http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041

- Integrate V_{in} for fixed time, de-Integrate with V_{ref} applied → $T_{De\text{-}Int} \sim V_{in}/V_{ref}$
- Insensitive to most linear error sources

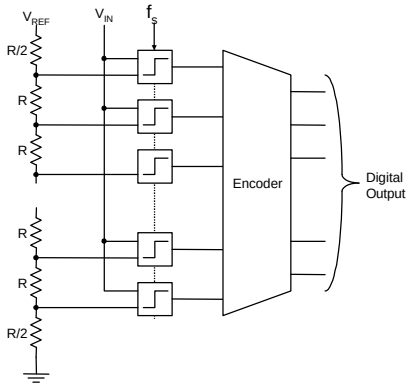
Successive Approximation



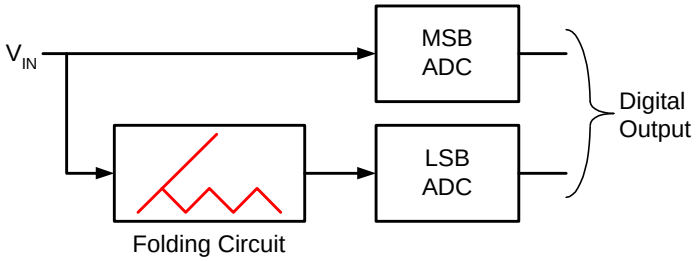
- Binary search over DAC output
- High accuracy achievable (16+ Bits)
- Moderate speed proportional to B (MHz range)

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance

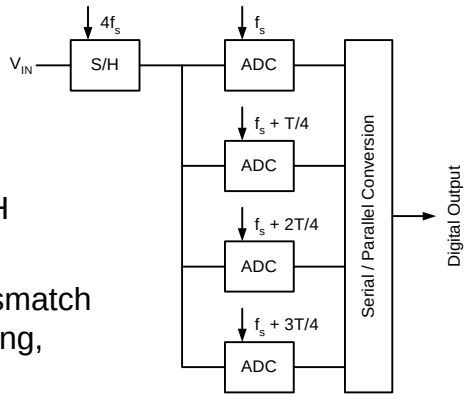


Folding Converter



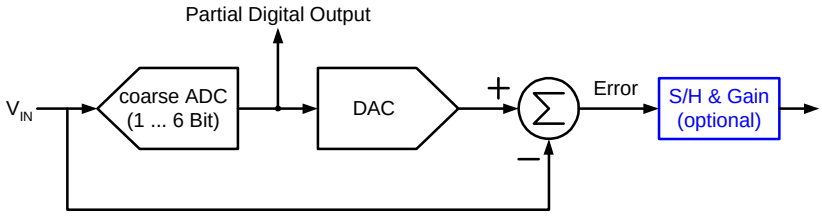
- Significantly fewer comparators than flash
- Fast
- Nonidealities in folder limit resolution to ~10Bits

Time Interleaved Converter



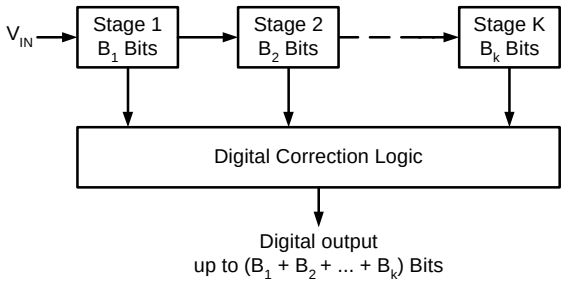
- Extremely fast:
  Limited by speed of S/H
- Accuracy limited by mismatch in individual ADCs (timing, offset, gain, …)

Residue Type ADC



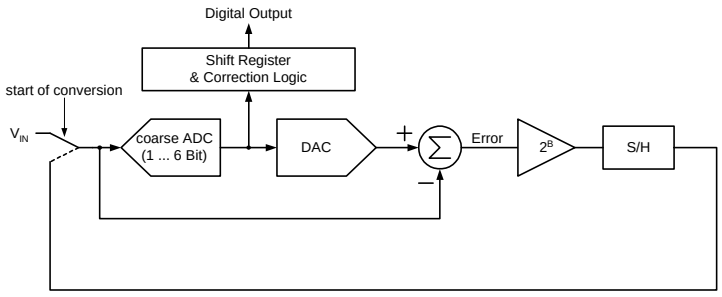
- Quantization error output (“residuum”) enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, …
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency

Pipelined ADC



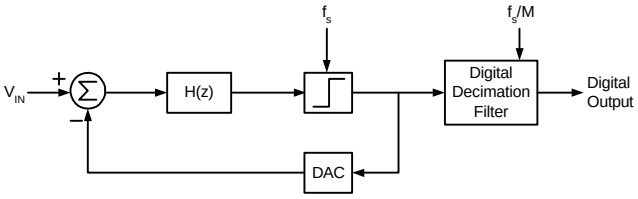
- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits / 1MS/s to 14Bits / 100MS/s

Algorithmic ADC



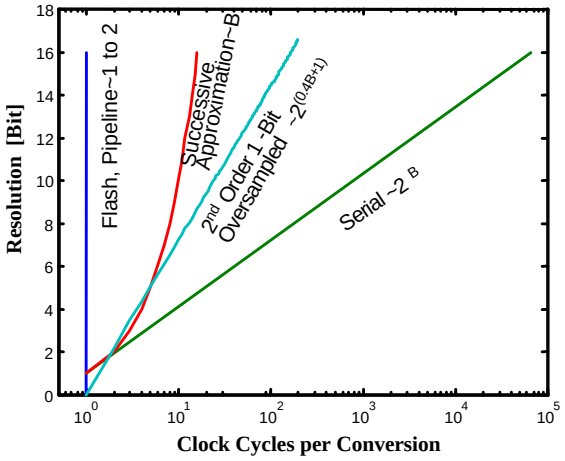
- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion

Oversampled ADC

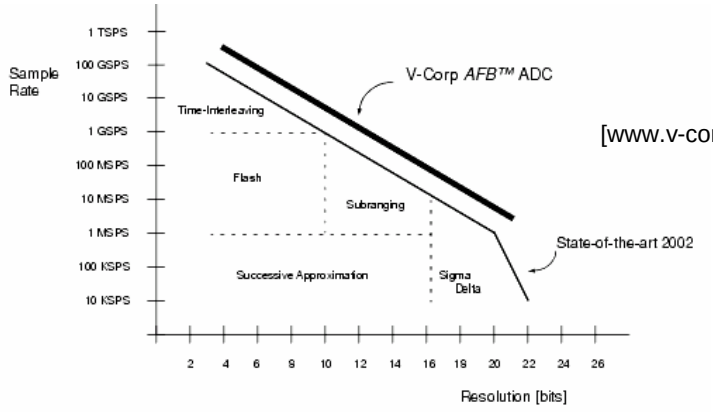


- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

Throughput Rate Comparison



Speed-Resolution Map



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