EE247
Lecture 24

- Administrative
  - EE247 Final exam:
    - Date: Wed. Dec. 15th
    - Time: -12:30pm-3:30pm-
    - Location: 289 Cory

    - Closed book/course notes
    - No calculators/cell phones/PDAs/Computers
    - Bring one 8x11 paper with your own notes
    - Final exam covers the entire course material

EE247
Lecture 24

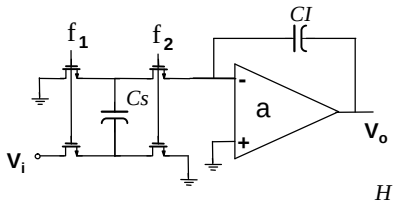
- Oversampled ADCs
  - 2nd order ΣΔ modulator
    - Practical implementation
      - Effect of various nonidealities on the ΣΔ performance
- Higher order ΣΔ modulators
  - Cascaded modulators (multi-stage)
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path

Oversampled ADCs
Last Lecture

- Oversampled ADCs
  - 1st order ΣΔ modulator
    - Quantization error
    - SQNR analysis
    - Limit cycle oscillation
  - 2nd order ΣΔ modulator
    - Dynamic range
    - Practical implementation
      - Effect of various nonidealities on the ΣΔ performance

2nd Order ΣΔ

Effect of Integrator Finite DC Gain

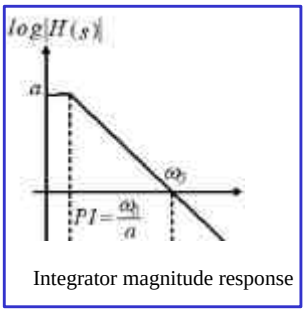


$$H(z)_{ideal} = \frac{Cs}{CI} \times \frac{z^{-1}}{1 - z^{-1}}$$

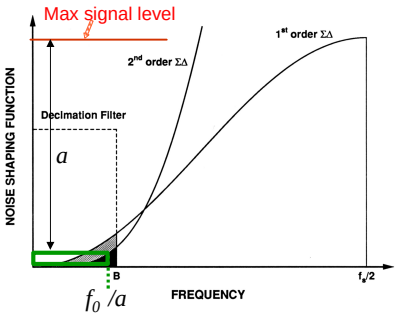
$$H(z)_{Finit\,DC\,Gain} = \frac{Cs}{CI} \times \frac{\left(\frac{a}{1 + a + \frac{Cs}{CI}}\right) z^{-1}}{1 - \left(\frac{1 + a}{1 + a + \frac{Cs}{CI}}\right) z^{-1}}$$

2nd Order ΣΔ

Effect of Integrator Finite DC Gain



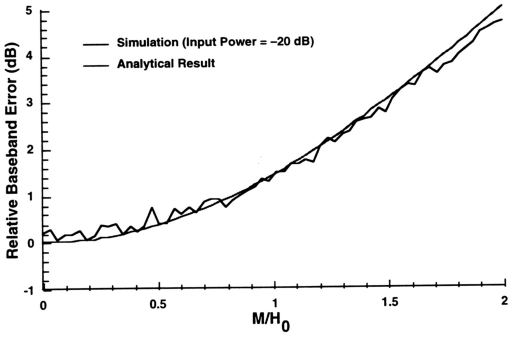
Integrator magnitude response



- Low integrator DC gain → degrades noise performance
- If a>M (oversampling ratio) → Insignificant degradation in SNR
- Normally DC gain designed to be >> M in order to suppress nonlinearities

2nd Order ΣΔ

Effect of Integrator Finite DC Gain

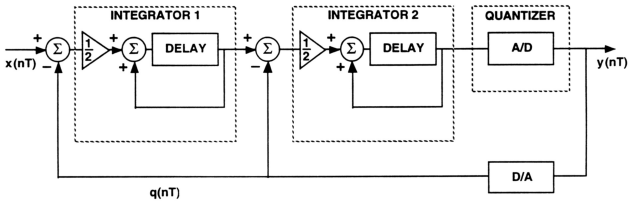


- Simulation results
- H_0=a → finite DC gain
- a> M → no degradation in SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

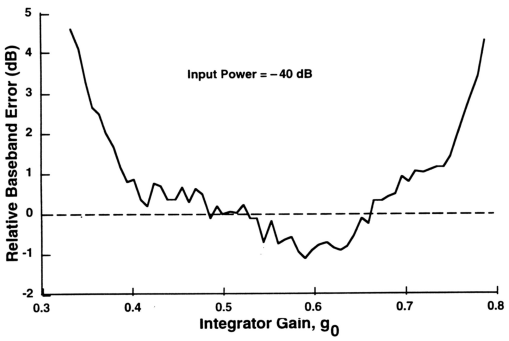
Effect of Integrator Overall Integrator Gain Inaccuracy



- Gain of ½ in front of integrators is a function of C1/C2 of the integrator
- The effect of C1/C2 inaccuracy inspected by simulation

2nd Order ΣΔ

Effect of Integrator Overall Gain Inaccuracy

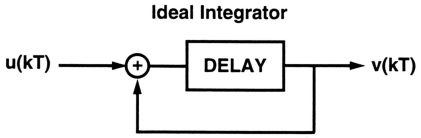


- Simulation show gain can vary by 20% w/o loss in performance
  → Confirms insensitivity of ΣΔ to component variations
- Note that for gain >0.65 system becomes unstable & SNR drops rapidly

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Nonlinearities



$$v(kT + T) = u(kT) + v(kT)$$

with nonlinearity

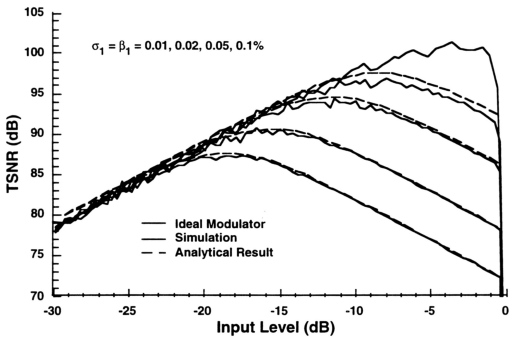
$$v(kT + T) = u(kT) + \alpha_1[u(kT)]^2 + \alpha_2[u(kT)]^3 + \ldots$$

$$+ v(kT) + \beta_1[v(kT)]^2 + \beta_2[v(kT)]^3 + \ldots$$

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Nonlinearities

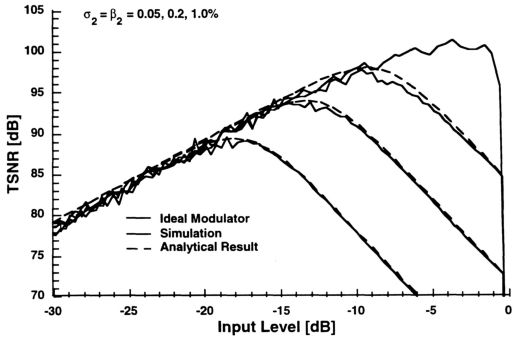


- Simulation for single-ended topology
- Even order nonlinearities can be significantly attenuated by using differential circuit topologies

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Nonlinearities

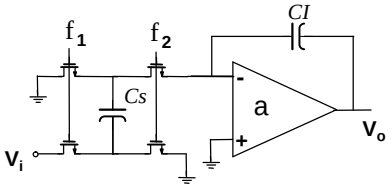


- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of KT/C noise



$$\overline{v^2_n} = 2\frac{KT}{Cs}$$

$$\overline{v^2_n}/f = 2\frac{kT}{Cs}\times\frac{1}{fs/2} = 4\frac{kT}{Cs\times fs}$$

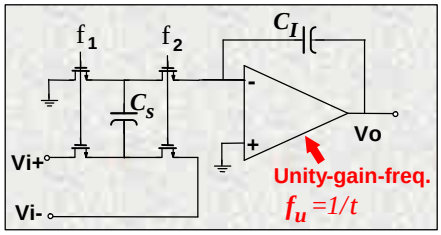
Total in-band noise:

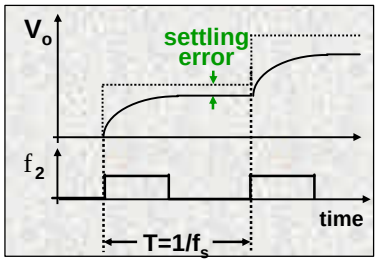
$$\overline{v^2_{n\,input}} = 4\frac{kT}{Cs\times fs}\times B$$

$$= \frac{2kT}{Cs\times M}$$

- For the example of digital audio with 16-bit (100dB) & M=256
  - → Cs=1pF → 6μVrms noise
  - →If FS=4$V_{p\text{-}p\text{-}d}$ then noise is -107dB → almost no degradation in overall SNR
  - →Cs=1pF, CI=2pF → small cap area compared to Nyquist ADC caps
  - →Since thermal noise provides some level of dithering → better not choose much larger capacitors!

2nd Order ΣΔ
Effect of Finite Opamp Bandwidth



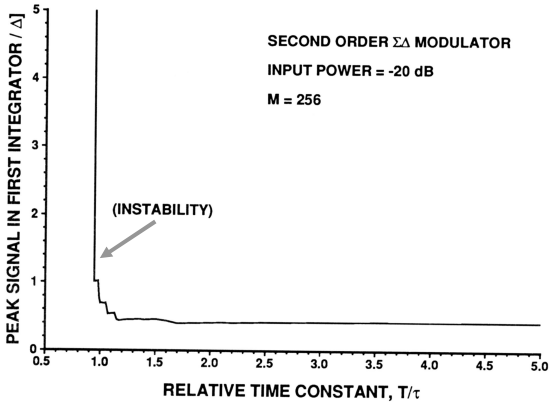


Assumption-

Opamp → does not slew

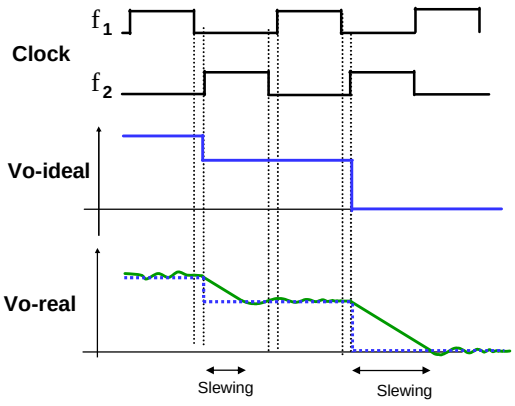
Opamp has only one pole → exponential settling

2nd Order ΣΔ
Effect of Finite Opamp Bandwidth

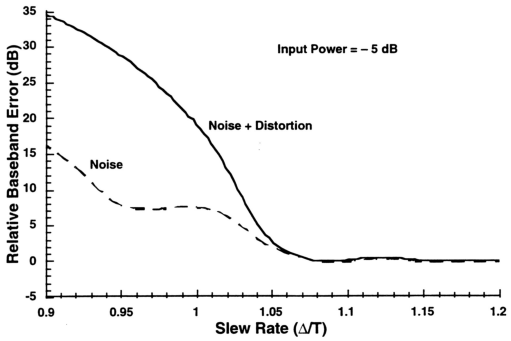


→ ΣΔ does not require high opamp bandwidth $f_u > 2f_s$ adequate

2nd Order ΣΔ
Effect of Slew Limited Settling



2nd Order ΣΔ
Effect of Slew Limited Settling



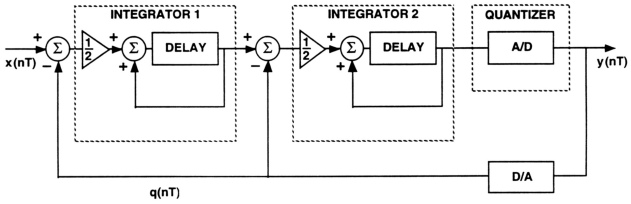
Assumption-

Opamp settling → slew limited

→Minimum slew rate of 1.2 (Δ x f_s) required

→Low slew rate degrade SNR rapidly

2nd Order ΣΔ
Effect of Comparator Non-Idealities on SD Performance

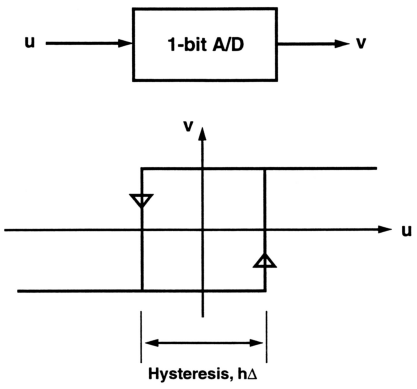


1-bit A/D → Single comparator

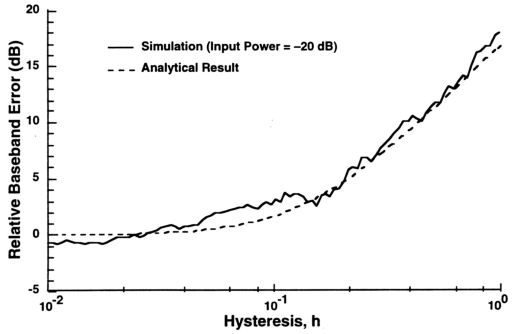
- •Speed must be adequate for the operating sampling rate
- •Input referred noise- same as offset
- •Input referred offset- feedback loop suppresses the effect → ΣΔ performance not sensitive to input referred offset
- •Hysteresis= Minimum overdrive required to change the output

2nd Order ΣΔ
Comparator Hysteresis

Hysteresis= Minimum overdrive required to change the output



2nd Order ΣΔ
Comparator Hysteresis



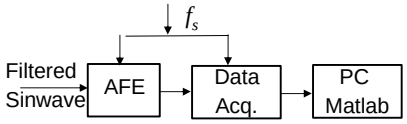
→ Comparator hysteresis < Δ/40 does not affect SNR
→ E.g. Δ=1V, comparator hysteresis up to 25mV tolerable

Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces
- SPICE type simulators normally used to test for gross circuit errors only
- SPICE type simulators too slow and not accurate enough for performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities as possible simultaneously to verify whether there are interaction among non-idealities

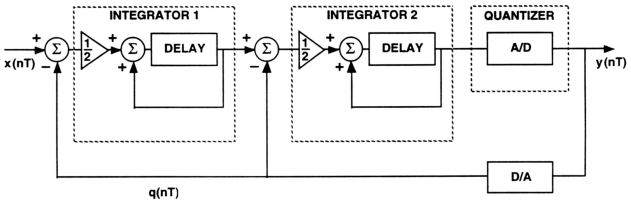
Modulator Testing

- Should make provisions for testing the modulator (AFE) separate from the decimator (digital back-end)
- Data acquisition board used to collect 1-bit digital output at fs rate
- Analyze data in a PC or dedicated test equipment in manufacturing environments can be used
- Need run DFT on the data and also make provisions to perform the function of digital decimation filter in software
- Typically, at this stage, parts of the design phase behavioral modeling effort can be utilized
- Good testing strategy vital for debugging/improving challenging designs



2nd Order ΣΔ

Implementation Example: Digital Audio Application



•5V supply, Δ=4Vp-p-d
•Minimum capacitor values computed based on noise -107dB wrt maximum signal
→ Max. inband KT/C noise =7*mVrms*
→ $C1=(2kT)/(M\ v_n^2)=1pF \quad C2=2C1$

Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications

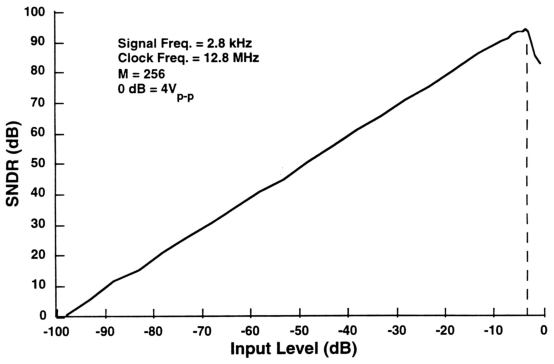
Summary of Measured Performance

Dynamic Range	**98 dB (16 bits)**
Peak SNDR	**94 dB (0.002% THD)**
Nyquist rate	**50 kHz**
Sampling rate	**12.8 MHz**
Oversampling Ratio	**256**
Differential input range	**4 V**
Supply voltage	**5 V**
Supply rejection	**60 dB**
Power dissipation	**13.8 mW**
Active Area	**0.39 mm^2**
Technology	**1-μm CMOS**

Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

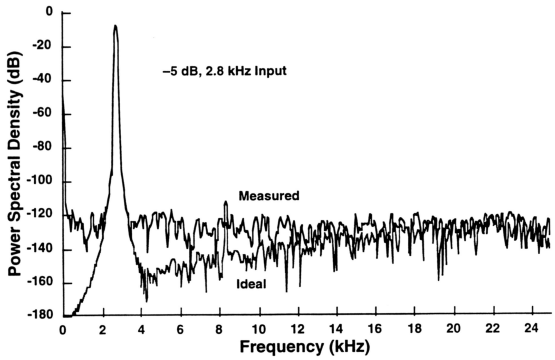
2nd Order ΣΔ
Implementation Example: Digital Audio Applications

Measured SNDR



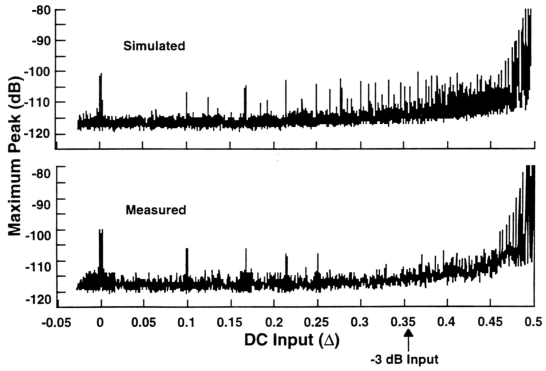
Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications



Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

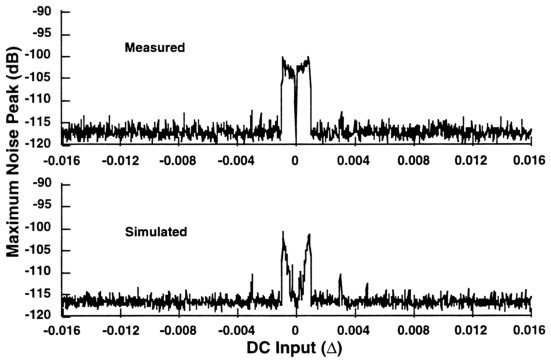
2nd Order ΣΔ
Implementation Example: Digital Audio Applications



→ Measured & simulated noise tone performance as a function of DC input signal
→ Sampling rate=12.8MHz, M=256

Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

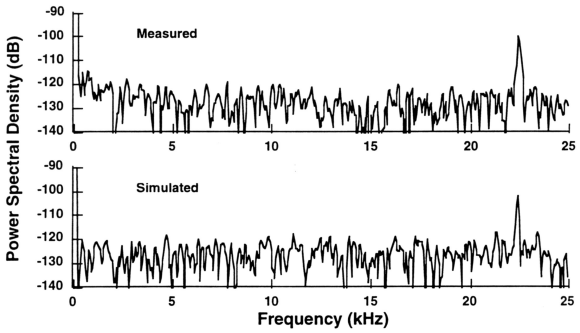
2nd Order ΣΔ
Implementation Example: Digital Audio Applications



→ Measured & simulated noise tone performance for near zero DC input
→ Sampling rate=12.8MHz, M=256

Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Digital Audio Applications

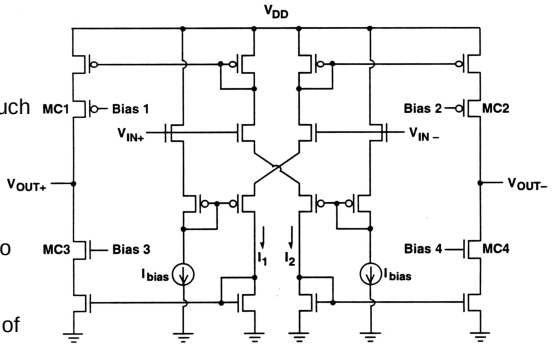


→ Measured & simulated worst-case noise tone @ DC input of 0.00088Δ
→ Sampling rate=12.8MHz, M=256

Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Integrator Opamp

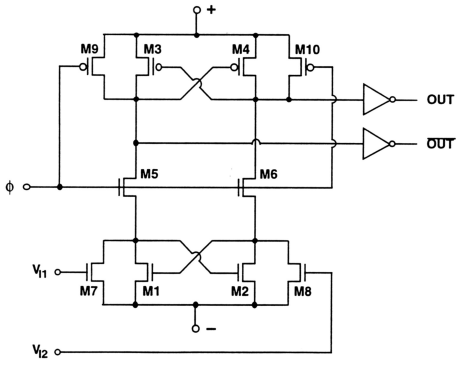
- Class A/B opamp + S.C. common-mode feedback
  → high slew-rate
- Input referred noise (both thermal and 1/f) should be much smaller compared to in-band quantization noise
- Minimum required DC gain M=256 , usually DC gain designed to be much higher to suppress nonlinearities
- Minimum required slew rate of 1.2(Δfs) → 65V/usec
- Minimum opamp settling time constant → 1/2fs~30nsec



Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Comparator

- Comparator → simple design
- Minimum acceptable hysteresis or offset → $\Delta/40 \sim 100mV$



Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2nd Order ΣΔ
Implementation Example: Subcircuit Performance

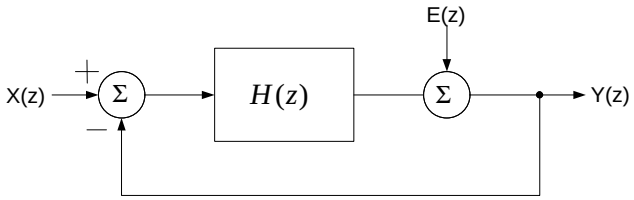
Subcircuit Performance		Our computed minimum required	Over-Design Factor
Operational Amplifier			
DC gain	**67 dB**	DC Gain 48dB	x8
Unity-gain frequency	**50 MHz**	Unity-gain freq =2fs=25MHz	x2
Slew rate	**350 V/μsec**	Slew rate = 65V/usec	x5
Linear output range	**6 V**	Output range 1.7Δ=6.8V!	X0.9
Sampling rate	**12.8 MHz**		
Integrator			
Settling time constant	**7.25 nsec**	Settling time constant= 30nsec	x4
Comparator			
Offset	**13 mV**	Comparator offset 100mV	x7

Ref: B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

Higher Order ΣΔ Modulators

- Two different architectural approaches used to implement ΣΔ modulators of order >2
  - Cascaded modulators (multi-stage)
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path

Higher Order ΣΔ Modulators
Mult-Stage Filter



$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z)$$

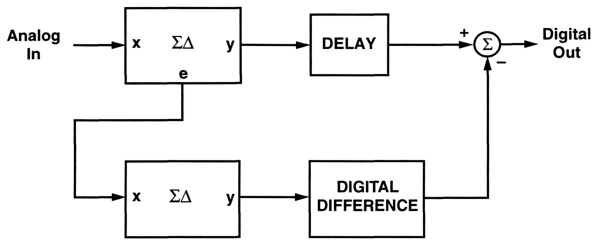
$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

- Zeros of NTF (poles of A(z)) can be positioned to flatten baseband noise spectrum
- Main issue → Loop stability for 3rd and higher orders

Higher Order ΣΔ Modulators
Cascaded Modulators

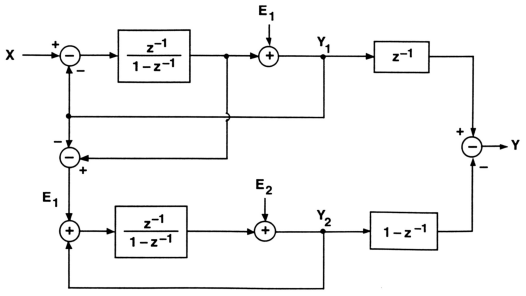
- Cascade two or more stable SD stages
- Quantization error of each stage is quantized by the succeeding stage and subtracted digitally
- Order of noise shaping equals sum of the orders of the stages
- Quantization noise cancellation depends on the precision of analog signal paths
- Typically, no potential instability

2-Stage Cascaded ΣΔ Modulators



- Main ΣΔ quantizes the signal
- The quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain

2nd Order (1-1) Cascaded ΣΔ Modulators



$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$$

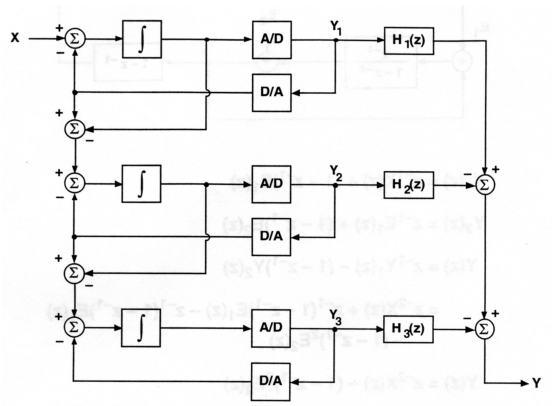
$$= z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z) - (1 - z^{-1})^2E_2(z)$$

$$\boxed{Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)}$$

2nd order noise shaping

3rd Order Cascaded ΣΔ Modulators

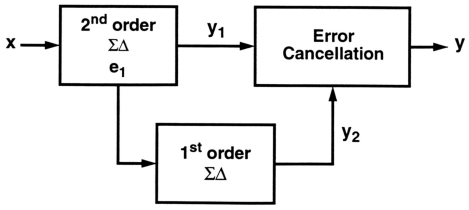
- Can implement 3rd order noise shaping with 1-1-1
- This is also called MASH



3rd Order (2-1) Cascaded ΣΔ Modulators

Advantages of 2-1 cascade:

- Low sensitivity to precision of analog paths
- Low spurious noise tones
- No potential instability



$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

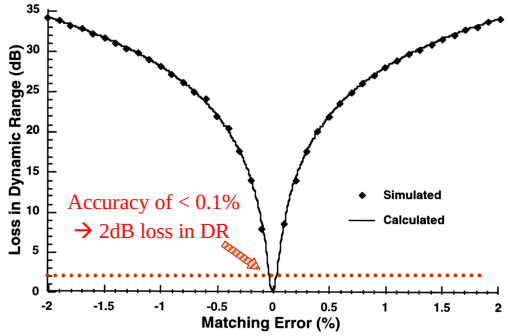
$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z)$$

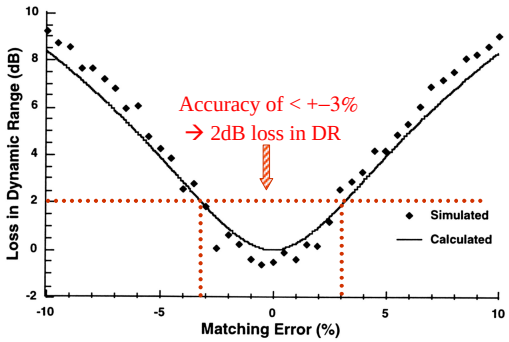
$$= z^{-3}X(z) + z^{-1}(1 - z^{-1})^2 E_1(z) - z^{-1}(1 - z^{-1})^2 E_1(z) - (1 - z^{-1})^3 E_2(z)$$

3rd order noise shaping ⟹ $\boxed{Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z)}$

Sensitivity of (1-1-1) Cascaded ΣΔ Modulators to Matching of Analog & Digital Gains



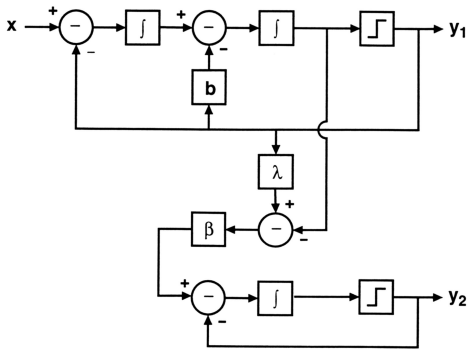
Sensitivity of (2-1) Cascaded ΣΔ Modulators to Matching Error



Main advantage of 2-1 cascade compared to 1-1-1 topology:

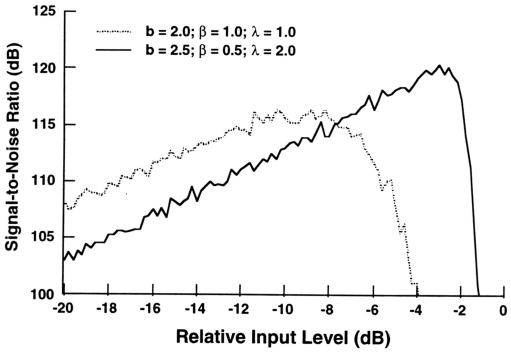
- Low sensitivity to precision of analog paths (over one order of magnitude!)

2-1 Cascaded ΣΔ Modulators



Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

2-1 Cascaded ΣΔ Modulators

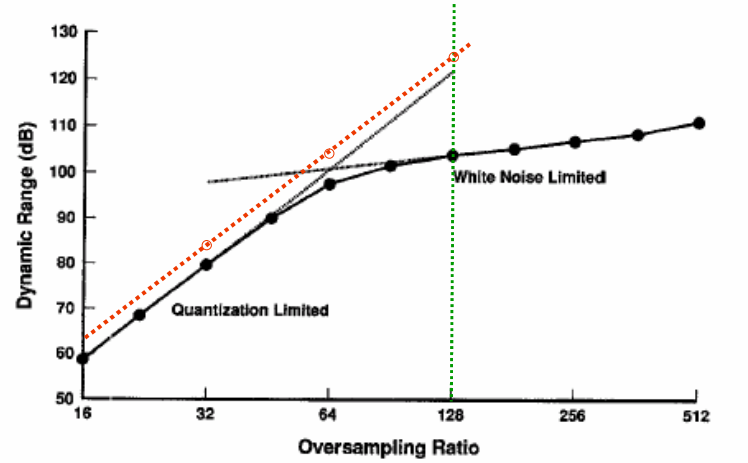


Effect of gain parameters on signal-to-noise ratio

Comparison of 2nd order & Cascaded (2-1) ΣΔ Modulator

Digital Audio Application, F_N=50kHz		
Reference	Brandt ,JSSC 4/91	Williams, JSSC 3/94
Architecture	2nd order	(2+1) Order
Dynamic Range	98dB (16-bits)	104dB (17-bits)
Peak SNDR	94dB	98dB
Oversampling rate	256	128
Differential input range	4Vppd 5V supply	8Vppd 5V supply
Power Dissipation	13.8mW	47.2mW
Active Area	0.39mm2	5.2mm2

2-1 Cascaded ΣΔ Modulators
Measured Dynamic Range Versus Oversampling Ratio



Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

Summary

- Oversampled ADCs decouple SQNR from circuit complexity and accuracy
- If a 1-Bit DAC is used, the converter is inherently linear—independent of component matching
- Typically, used for high resolution & low frequency applications – e.g. digital audio
- 2nd order ΣΔ used extensively due to lower levels of limit cycle related spurious tones
- ΣΔ modulators of order greater than 2:
  - –Single-loop, single-quantizer modulators with multi-order filtering in the forward path
  - –Cascaded (multi-stage) modulators

Refs:

J. C. Candy and G. C. Temes, "Oversampling Methods for A/D and D/A Conversion", Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation, 1992, pp. 1-25.

S. R. Norsworthy, R. Schreier, and G. C. Temes, "Delta-Sigma Data Converters, Theory, Design, and Simulation," IEEE Press, 1997.