University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 150 R. Katz
Fall 2000 N. Zhou

Checkpoint 4
Packet Transmission Reception

1 Objective

For this checkpoint you will make additions to your UART design from checkpoint 2 so that you can transmit and receive packets according to the protocol defined for this semester's 150 project.

2 Protocol Details

For this project we will define a packet as a series of 5 UART transmissions. The first byte of a transmission is called the header, the four remaining bytes will be the data of the transmission, in this case it will be four samples of audio waveform.

In the header byte bits 7,6 are control bits, which are zero for all normal packets. (You may use these bits to extend the protocol to introduce extra features for extra credit in the final project) bits 5,4,3 are the destination of a transmission, and bits 2,1,0 are the source of the transmission.
(See my power point slides for illustration of a packet)

The procedure for transmitting a packet is as follows:

1. Always listen to what is happening on the shared bus. This means that the RX unit receives all transmissions on the shared line, including your own transmission.
2. Start transmission only after a random waiting period after the bus becomes idle. The bus is considered idle if there as been 16 consecutive '1' at 250KHz or immediately after a packet transmission.
3. If two stations happen to start a transmission at the same time then the transmission that has the first 0 in the transmission wins. (Notice a transmission should never interrupt the middle of another transmission because once the start bit is detected for the first transmission the bus is not idle anymore)
4. The winner goes on transmitting as if nothing was wrong.
5. The loser notices that a collision has happened, stops transmission immediately, and goes back to step 2 to try again later.

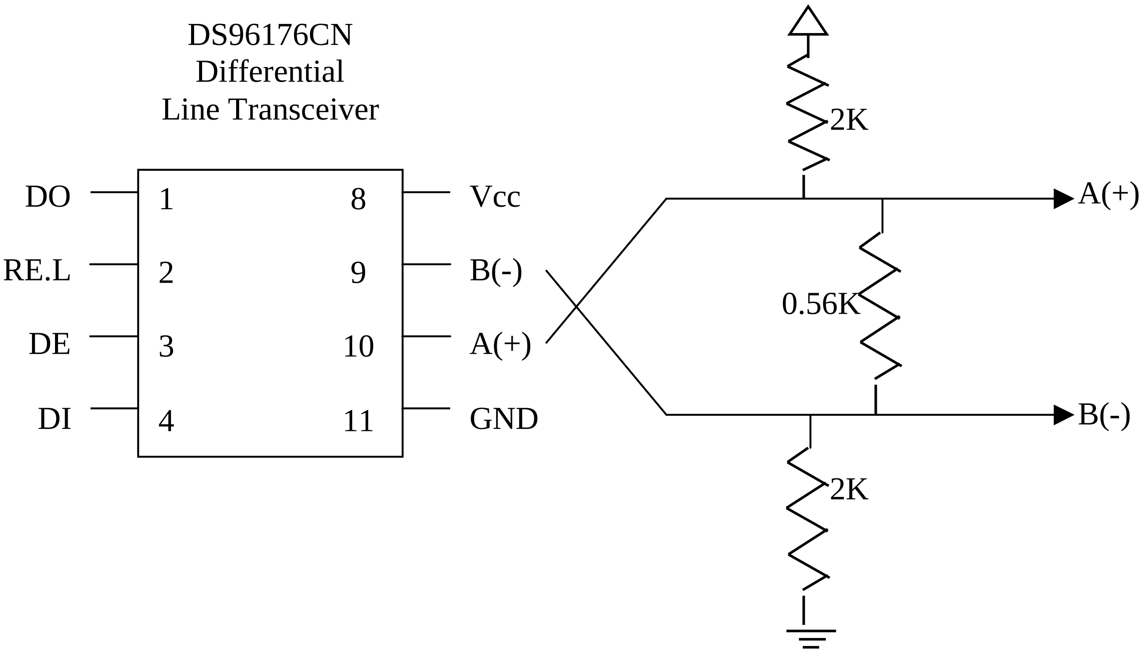
3 Wiring

For this checkpoint you will receive one chip (DS96176CN Differential Line Transceiver), one discrete package with 3 resistors on it, and a 7ft twisted pair wire for connecting different stations. The wiring should be done as follows: (**you will need to invert your TX from your UART to get TX.L**)

DS96176CN	**FPGA**
DO pin1	RX
RE.L pin2	GND
DE pin3	TX.L
DI pin4	GND

Correction

A(+) and B(-) should be wire-wraped to 2 consecutive pins on the board so that you can plug in the twisted pair wires.



Important: because TX.L is wired into the DE the transceiver only actively drives a ‘0’ onto the bus. The resistors are used to passively pull the bus to a ‘1’ when nothing is driving. This means that when the TX from different boards different values, ‘0’ always wins. This is very important for figuring out collisions and is also the reason why the transmission with the first ‘0’ wins the collision.

4 Your design.

For this checkpoint you are expected to design an implementation of the packet communication protocol described earlier. Your design should transmit one packet each time the SPARE button is pushed. The header of the packed should be taken from the dipswitches. The four data bytes can be arbitrarily chosen (for ease of testing you should choose 4 different numbers). There will be a provided bit file for testing your logic design. You can use your UART bit file from chkpt2 to test your physical wiring.

Specs for the provided bit file:
a) The provided bit file will attempt to transmit one packet every 2KHz.
b) The header for the packet being transmitted packet is all ‘0’.
c) The data packet contains the “secret” message.
d) The provided bit file has a zero random wait time, so on a “coin toss” it always wins.
e) The provided bit file filters out any packet with destination of ‘000’. (Ignores it’s own transmissions)
f) The spare button chooses which byte from the four data bytes of a received packet to display.

Specs expected for your design:
a) Transmit one packet every time SPARE is pushed. The header of the packet should come from the DIPSWITCH.
c) Correctly waits for the bus to be idle and correctly implement pseudo-random wait time before starting transmission. **Use (6 bits of a 2MHz 8 bit LFSR) = ([5:0] Header Byte) as the random start time.**
d) Correctly implements collision detection and back off.
f) Correctly detects the idle state of the bus, 16 ‘1’s, or immediately after a completed packet. (Note there should never be 16 ‘1’s in the middle of a packet, if it does happen that means something went wrong and the current packet should be aborted)
g) Correctly receives packets from the bus, and latches the data portions of the packet into display registers after reception of a completed packet. (You do not need to do any filtering of the packets for destination check for this checkpoint)
b) Switch which byte of received packet to display every time SPARE is pushed.

Testing:

For testing your design:

a) Load your compiled bit file onto one board.
b) Load the provided bit file to another board.
c) Connect the A(+), B(-) of the 2 boards with the twisted pair wires.
d) If all goes well your design should display the “secret” message from the provided bit file, and the provided bit file will display your transmission.

Name________________________________ Name________________________________

Lab Section (Check one)

M: ☒ AM T: ☒ AM W: ☒AM Th:

☒ PM ☒ PM ☒PM ☒PM

Checkpoint 4 Check-offs

- Explain the network protocol to a TA

TA: ____________________ (10%)

- Show your schematics to a TA and explain your DATAPATH and how it functions.

TA: ____________________ (10%)

- Show and explain some representation of the FSM you have designed to generate the control signal for your DATAPATH.

TA: ____________________ (10%)

- Verify that your design works by showing that you can receive your own packet.

TA: ____________________ (10%)

- Verify your design with another board loaded with the TA bit file.

TA: ____________________ (50%)

- Use the digital analyzer to show that your design indeed does wait for the bus to be idle before transmission.

TA: ____________________ (10%)

Turned in on time TA: ____________________ (×100%)

Turned in 2 week late TA: ____________________ (×50%)